New XC9500 CORE Support

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Xilinx CPLDs offer you a number of advantages such as high system clock speeds, short pin-to-pin delays, industry standard JTAG support, and non-volatile FLASH-based In-System Programmability (ISP). Xilinx XC9500 CPLDs are perfect for integrating many off-the-shelf ICs, and because you can easily customize or enhance any design, CPLDs offer you the ability to optimize your system for speed, density, cost, or all three. Now, you also have the time-to-market and ease-of-use advantages of intellectual property (cores) as well.

There are three ways you can take advantage of XC9500 devices using COREs:

- **LogiBLOX** - The XC9500 family is now fully supported by the LogiBLOX module generator in the new Alliance Series and Foundation Series 1.5 release, shipping this summer.
- **AllianceCORE** - The XC9500 family is also supported under the Xilinx AllianceCORE program. Core designs for UARTs, MicroProgram Controllers, Peripheral Interface Controllers, DRAM Controllers, and Synchronous DRAM Controllers are available today.
- **Xilinx CORE Generator** - XC9500 functionality and support will be incorporated into the Xilinx CORE Generator in the first half of 1999.

Simplifying the design process through the use of proven, high-performance cores gives you significant benefits. Now, Xilinx adds the XC9500 ISP CPLD family to the list of core-compatible device architectures that help you achieve higher performance results with significant reductions in design time. ◆