Mixed Schematic and HDL Design Entry

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HDL VERIFICATION SPECIAL SECTION

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Xilinx allows complete design flexibility. Even though a significant amount of designs are done totally in schematics or HDL, there is also an ability to mix these two popular entry methods. With a top-level HDL or schematic, the submodules can be either HDL or schematics. The advantages to mixed-mode design entry are:

- Flexible design environment for a design team with mixed skill members. (Some are skilled in schematics while others are skilled in HDL.)
- You can use existing schematic designs.
- Allows a visual representation of large logic blocks and interconnect via a top-level schematic.
- HDL descriptions of large blocks are easier to understand, and simulate quickly and easily.
- You have total control of logic mapping and constraints in a schematic.
- You can automatically optimize and map an HDL design using synthesis tools.

A mixed mode design can be simulated, with a top-level HDL or schematic, at the following five stages of your design cycle:

1. Before synthesis.
2. After synthesis.
3. After the Translate step in the Flow Engine.
4. After the Map step in the Flow Engine.
5. After the Place & Route step in the Flow Engine.

Simulation with a Schematic at the Top Level

1. Before synthesis, instantiate HDL modules into the schematic and simulate the schematic using test vectors. The HDL modules are simulated for functionality before synthesis using an HDL testbench. It is also possible to simulate the complete design using appropriate simulation tools. In the Mentor design environment, you can use QuickHDL Pro to co-simulate schematics and HDL. In the Cadence design environment, you can use Verilog XL to simulate the complete design by merging the pre-synthesis HDL modules with the gate level HDL netlist written by Concept.
2. After synthesis, generate an EDIF netlist for the HDL modules. In the Mentor design environment, you can merge schematic EDIF netlists and HDL EDIF netlists, and simulate the complete design using Quicksim, which is a schematic gate-level simulator. In the Cadence design environment, you can re-simulate the design using Verilog XL after synthesis by writing a post-synthesis HDL netlist merged with the gate level HDL netlist written by Concept.
3. After translate, create an EDIF file by running NGD2EDIF from the command line to re-simulate the gate level netlist after translation to Xilinx primitives.
4. After map and before place and route, simulate your design with block delays but not routing delays. Use NGDANNO from the command line to create a back annotated simulation file and use NGD2EDIF to create an EDIF file. You can

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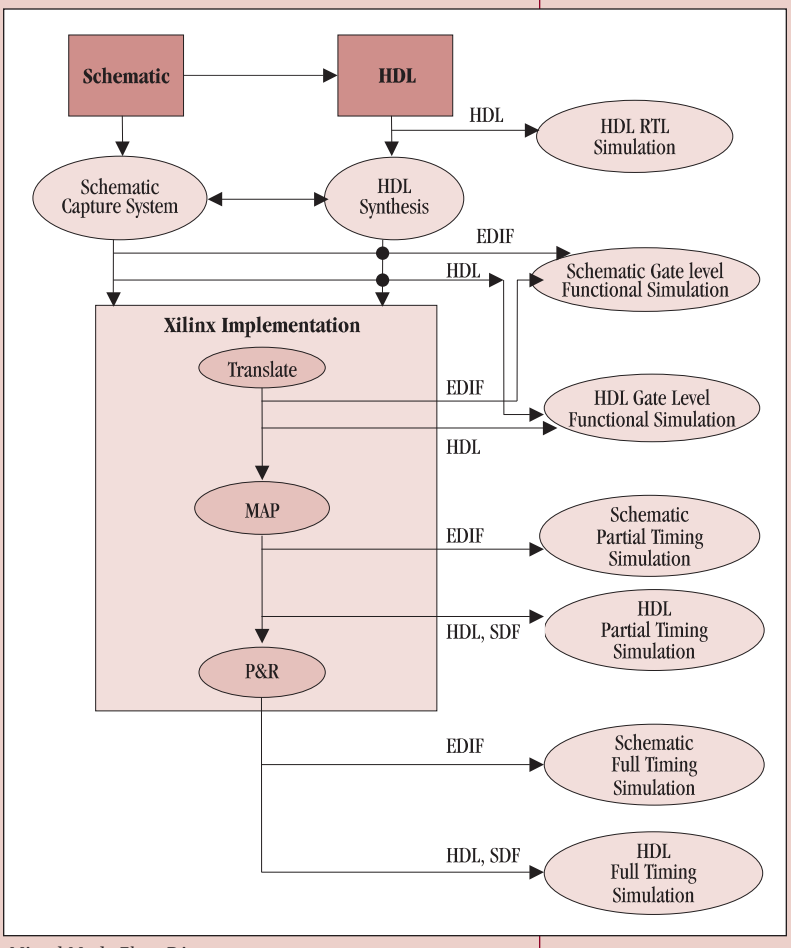

Mixed Mode Flow Diagram

then perform timing simulation with block delays. This is generally a good way to test whether the design is meeting your timing requirements before spending the time to do a full place and route.

5. After place and route (if you have previously selected EDIF as the simulation data format), simulate your complete design with both block and routing delays.

Simulation with an HDL at the Top Level

1. Before synthesis, simulate the HDL modules of your design using an HDL testbench. You can simulate schematic components using a gate level simulator. You can simulate the complete design as in the case of a top-level schematic.
2. After synthesis, generate an EDIF netlist for the HDL modules. You can simulate the gate level function of the complete design as in the case of a top-level schematic.
3. After translate, generate a structural HDL netlist using NGD2VER or NGD2VHDL for gate level simulation after the design is translated to Xilinx primitives.
4. After map, simulate the design with block delays similar to a top-level schematic except using the command line NGD2VHDL or NGD2VER to create a structural simulation netlist.
5. After place and route, (if you have previously selected VHDL or Verilog as the simulation data format), simulate the complete design with both block and routing delays with VHDL/Verilog and associated SDF (standard delay format) file.

Bus Notation in Schematic and in Synthesis

In a mixed mode design, the Bus Dimension Separator style in your schematic must match your synthesis bus style. If you use a synthesis option to generate one bus style and then use the EDIF from your schematic to generate a different bus style, the implementation tool will not merge the schematic module with the rest of the design, leaving it unexpanded.

Conclusion

Xilinx allows mixed mode design methodology with both HDL and schematic submodules. With a schematic at the top level, you can reuse test vectors throughout the design cycle; while with HDL at the top level, you can reuse your testbench throughout the design. ◆