TECHNICAL SEMINAR

X-Fest 2K is a nationwide technical seminar series designed to educate and inform both advanced and new users of Xilinx programmable logic. Ten highly technical mini courses have been developed by Insight Electronics to provide attendees with concise solutions and practical examples of today's most challenging programmable logic design issues. Two course tracks have been created; one for new user's of programmable logic, and the second for current and advanced Xilinx designers. The new user's track offers three courses designed to explain and demonstrate the Xilinx design flow process from design entry, to simulation, fitting, and device programming. The advanced track offers three courses covering practical implementation tips for advanced FPGA features. From the Virtex and Spartan II DLL's, BlockRAM, and SelectI/O, to the multiple configuration options of JTAG, SelectMAP, MultiLINX, and SPROM, the advanced courses help simplify your options.

X-FEST 2K

To reserve your spot or to ask additional questions about this seminar call 1.800.677.7716 in the U.S or 1.800.204.0010 in Canada.

LOCATIONS & SCHEDULE

San Diego	February 11	Chicago	March 15	Austin	April 5
Los Angeles	February 15	Minneapolis	March 16	Huntsville	April 6
Orange County	February 16	Portland	March 17	Raleigh	April 7
San Jose	February 17	Atlanta	March 21	New York	April 11
Montreal	February 23	Orlando	March 22	Connecticut	April 12
Ottawa	February 24	Ft. Lauderdale	March 23	Rochester	April 13
Toronto	February 25	Tampa	March 24	New Jersey	April 18
Phoenix	February 29	Salt Lake City	March 28	Philadelphia	April 19
Dallas	March 1	Calgary	March 29	Cleveland	May 2
Denver	March 2	Boston	March 30	Detroit	May 3
Seattle	March 3	Vancouver	March 30	Ft. Wayne	May 4
Baltimore	March 14	Houston	April 4	Dayton	May 5

Insight

Insight Electronics, LLC ▪ United States 800.677.7716 ▪ Canada 800.204.0010 ▪ Mexico 525.488.0119
Brazil 011.5511.5505.6501 ▪ Argentina 011.5411.4735.2659 ▪ http://www.insight-electronics.com

COURSE SCHEDULE

8:00 – 8:30	Registration and Continental Breakfast	
8:30 – 8:45	Welcome and Introduction	
8:45 – 9:30	Xilinx Product Update	
9:30 – 10:30	On-Chip Debugging	
10:30 – 10:45	BREAK	
10:45 – 11:45	Systematic Approach to High Performance FPGA Design	The New Xilinx CoolRunner Family
11:45 – 1:00	LUNCH – The Future of Programmable Logic	
1:00 – 2:00	Leveraging Advanced Features of Virtex and Spartan II	Xilinx Design Flow I
2:00 – 2:15	BREAK	
2:15 – 3:15	Improving Timing Performance – Squeezing Those Last Nanoseconds	Xilinx Design Flow II
3:15 – 4:15	A Practical Guide to FPGA Configuration	Xilinx Design Flow III
4:15 – 4:30	Wrap-Up and Door Prizes	

COURSE DESCRIPTIONS

Xilinx Product Update Xilinx is leading the programmable logic industry with new device architectures, advanced software, and web based tools and training. This fast paced course will provide you with a general overview of these new device families, including Virtex-E, Spartan II, CoolRunner, and XC9500XV. New software solutions such as Team Design, Internet Reconfigurable Logic, and System Debug, will be presented, as well as Xilinx's advanced web-based tools and education offerings.

On-Chip Debugging Ever wish you could see what was really going on inside that FPGA chip? Well, now you can. This course will present some of Xilinx's new capabilities for on-chip verification and debug. Gain visibility to internal data buses and signals, capture data, and review the results. If you are designing with Virtex, Virtex-E, or Spartan II, you will instantly see how these tools will significantly cut your system integration and debug time.

Systematic Approach to High Performance FPGA Design Presented by Memec Design Services, this session will describe a design process and several techniques useful for getting the most performance from your FPGA silicon. While these techniques were developed for high-speed designs, they are useful for designs with high device utilization or designs attempting to maximize performance from slower, less expensive silicon. The design process is independent of your choice of design entry method and has been successfully used in schematic, HDL, and mixed design flows. The use of "black-boxes" such as cores or netlists is also addressed during this session.

The New Xilinx CoolRunner Family See the new Xilinx XPLA3 CPLD architecture, designed for low power applications based on CoolRunner Technology. Learn about the new architecture features that enhance performance and design flexibility, while delivering the industries lowest power CPLD solution. See a design flow example including design synthesis, device fitting, and in-circuit programming using industry standard JTAG. A comparison of the power and performance of the XPLA3 architecture versus other PAL type CPLDs will also be presented.

The Future of Programmable Logic Where will programmable logic be 5 years from now? See what Xilinx has planned for both silicon and software. This presentation will be given during lunch.

Leveraging Advanced Features of Virtex and Spartan II A practical course in how to utilize the sophisticated silicon structures in the Virtex, Virtex-E, and Spartan II family FPGAs. Literal examples will be given on how to implement and use the Block RAM for FIFOs, data storage and funneling data to different width/speed combinations. Illustrations will be presented on using the DLLs for chip and board level de-skewing, clock multiplication and division, as well as additional clocking features. The ability of these family members to interface to multiple I/O standards simultaneously, including LVDS, will be demonstrated with proven examples.

Improving Timing Performance - Squeezing Those Last Nanoseconds Presented by Synplicity, this course will teach you some of the more advanced techniques available for improving timing performance. Practical coding examples and methodologies will be covered along with tool demonstrations.

Practical Guide to FPGA Configuration This course will cover FPGA configuration from the basics of the serial configuration modes, to the more complex Virtex SelectMap modes. There also will be a discussion and demonstration of the latest programming cables, and some common configuration debugging techniques.

Xilinx Design Flow This series of three courses is designed to take the user through the entire Xilinx design process. Starting with design entry and finishing with device programming, these courses will address all aspects of the design flow process.

Design Flow I Understand the Xilinx tools offering and how they fit with 3rd party solutions. Learn the basics of the Foundation tool settings and options and see a demo.

Design Flow II This course will demonstrate the features of the Xilinx Design Manager. The attendee will learn the basics of the user interface, how to create projects, process designs, and analyze design timing. Two primary types of design flows will be shown: timing-driven, and non-timing driven. How and when to use the most appropriate flow will be discussed, as well as design flow options, and how to balance run-time and design performance. Achieving high-performance designs through the use of the Constraints Editor and Timing Analyzer utilities will be demonstrated. Advanced utilities such as the Floorplanner and FPGA Editor will also be introduced.

Design Flow III Building on Modules I and II, this course will present how to complete the design process by generating programming data and downloading designs for both FPGAs and CPLDs. Demonstrations on the JTAG and MultiLINX programming cables will be given along with an explanation of the Xilinx PROM File Formatter. The new ISP configuration PROM will also be explained.

- Exclusively sponsored by Insight Electronics
- Door prizes include MP3 Player, Golf Shirts, and Tee Shirts
- All attendees get a Seminar Booklet, CD, and Gifts

X-FEST 2K

- Free Lunch provided
- Discount Coupons for XILINX Foundation and Alliance software as well as Insight Scalable Solutions development kits

Insight's Center of Xcellence Xilinx Programmable Logic

Synplicity

Insight

Memec Design Services

XILINX