Virtex-E Electrical Characteristics

Definition of Terms

Data sheets may be designated as Advance or Preliminary. The status of specifications in these data sheets is as follows:

Advance: Initial estimates based on simulation and/or extrapolation from other speed grades, devices, or families. Values are subject to change. Use as estimates, not for production.

Preliminary: Based on preliminary characterization. Further changes are not expected.

Unmarked: Data sheets not identified as either Advance or Preliminary are to be considered final.

All specifications are representative of worst-case supply voltage and junction temperature conditions. The parameters included are common to popular designs and typical applications. Contact the factory for design considerations requiring more detailed information.

All specifications are subject to change without notice.

DC Characteristics

Absolute Maximum Ratings

Symbol	Description			Units
V_{CCINT}	Internal Supply voltage relative to GND		-0.5 to 2.0	V
V_{CCO}	Supply voltage relative to GND		-0.5 to 4.0	V
V_{REF}	Input Reference Voltage		-0.5 to 4.0	V
V_{IN}	Input voltage relative to GND		-0.5 to 4.0	V
V_{TS}	Voltage applied to 3-state output		-0.5 to 4.0	V
V_{CC}	Longest Supply Voltage Rise Time from 0 V - 1.71 V		50	ms
T_{STG}	Storage temperature (ambient)		-65 to +150	°C
T_{SOL}	Maximum soldering temp. (10 s @ 1/16 in. = 1.5 mm)		+260	°C
T_J	Junction temperature	Plastic packages	+125	°C

Notes: Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those listed under Operating Conditions is not implied. Exposure to Absolute Maximum Ratings conditions for extended periods of time may affect device reliability.

Power supplies may turn on in any order.

Recommended Operating Conditions

Symbol	Description		Min	Max	Units
V_{CCINT}	Supply voltage relative to GND, T_J = 0 °C to +85°C	Commercial	1.8 - 5%	1.8 + 5%	V
	Supply voltage relative to GND, T_J = -40°C to +100°C	Industrial	1.8 - 5%	1.8 + 5%	V
V_{CCO}	Supply voltage relative to GND, T_J = 0 °C to +85°C	Commercial	1.2	3.6	V
	Supply voltage relative to GND, T_J = -40°C to +100°C	Industrial	1.2	3.6	V
T_{IN}	Input signal transition time			250	ns

DC Characteristics Over Recommended Operating Conditions

Symbol	Description		Device	Min	Max	Units
V_{DRINT}	Data Retention V_{CCINT} Voltage (below which configuration data may be lost)		All	1.5		V
V_{DRIO}	Data Retention V_{CCO} Voltage (below which configuration data may be lost)		All	1.2		V
I_{CCINTQ}	Quiescent V_{CCINT} supply current (Note 1)		XCV50E			
			XCV100E			
			XCV200E			
			XCV300E			
			XCV400E			
			XCV600E			
			XCV1000E			
			XCV1600E			
			XCV2000E			
			XCV2600E			
			XCV3200E			
I_{CCOQ}	Quiescent V_{CCO} supply current (Note 1)		XCV50E			
			XCV100E			
			XCV200E			
			XCV300E			
			XCV400E			
			XCV600E			
			XCV1000E			
			XCV1600E			
			XCV2000E			
			XCV2600E			
			XCV3200E			
I_{REF}	V_{REF} current per V_{REF} pin		All			µA
I_L	Input or output leakage current		All			µA
C_{IN}	Input capacitance (sample tested)	BGA, PQ, HQ, packages	All			pF
I_{RPU}	Pad pull-up (when selected) @ V_{in} = 0 V, V_{CCO} = 3.3 V (sample tested)		All	Note 2		mA
I_{RPD}	Pad pull-down (when selected) @ V_{in} = 3.6 V (sample tested)			Note 2		mA

Note 1: With no output current loads, no active input pull-up resistors, all I/O pins Tri-stated and floatingNote 2:Internal pull-up and pull-down resistors guarantee valid logic levels at unconnected input pins. These pull-up and pull-down resistors do not guarantee valid logic levels when input pins are connected to other circuits.

DC Input and Output Levels

Values for V_{IL} and V_{IH} are recommended input voltages. Values for I_{OL} and I_{OH} are guaranteed output currents over the recommended operating conditions at the V_{OL} and V_{OH} test points. Only selected standards are tested. These are chosen to ensure that all standards meet their specifications. The selected standards are tested at minimum V_{CCO} with the respective V_{OL} and V_{OH} voltage levels shown. Other standards are sample tested.

Input/Output Standard	V_{IL}		V_{IH}		V_{OL}	V_{OH}	I_{OL}	I_{OH}
	V, min	V, max	V, min	V, max	V, Max	V, Min	mA	mA
LVTTL (Note 1)	- 0.5	0.8	2.0	3.6	0.4	2.4	24	- 24
LVCMOS2	- 0.5	0.7	1.7	3.6	0.4	1.9	12	- 12
LVCMOS18	- 0.5	20% V_{CCO}	70% V_{CCO}	1.95	0.4	V_{CCO} - 0.4	8	- 8
PCI, 3.3 V	- 0.5	30% V_{CCO}	50% V_{CCO}	V_{CCO} + 0.5	10% V_{CCO}	90% V_{CCO}	Note 2	Note 2
GTL	- 0.5	V_{REF} - 0.05	V_{REF} - 0.05	3.6	0.4	n/a	40	n/a
GTL+	- 0.5	V_{REF} - 0.1	V_{REF} + 0.1	3.6	0.6	n/a	36	n/a
HSTL I	- 0.5	V_{REF} - 0.1	V_{REF} + 0.1	3.6	0.4	V_{CCO} - 0.4	8	-8
HSTL III	- 0.5	V_{REF} - 0.1	V_{REF} + 0.1	3.6	0.4	V_{CCO} - 0.4	24	-8
HSTL IV	- 0.5	V_{REF} - 0.1	V_{REF} + 0.1	3.6	0.4	V_{CCO} - 0.4	48	-8
SSTL3 I	- 0.5	V_{REF} - 0.2	V_{REF} + 0.2	3.6	V_{REF} - 0.6	V_{REF} + 0.6	8	-8
SSTL3 II	- 0.5	V_{REF} - 0.2	V_{REF} + 0.2	3.6	V_{REF} - 0.8	V_{REF} + 0.8	16	-16
SSTL2 I	- 0.5	V_{REF} - 0.2	V_{REF} + 0.2	3.6	V_{REF} - 0.61	V_{REF} + 0.61	7.6	-7.6
SSTL2 II	- 0.5	V_{REF} - 0.2	V_{REF} + 0.2	3.6	V_{REF} - 0.80	V_{REF} + 0.80	15.2	-15.2
CTT	- 0.5	V_{REF} - 0.2	V_{REF} + 0.2	3.6	V_{REF} - 0.4	V_{REF} + 0.4	8	-8
AGP	- 0.5	V_{REF} - 0.2	V_{REF} + 0.2	3.6	10% V_{CCO}	90% V_{CCO}	Note 2	Note 2

Note 1: V_{OL} and V_{OH} for lower drive currents are sample tested.
Note 2: Tested according to the relevant specifications.

LVDS DC Specifications

DC Parameter	Conditions	Min	Typ	Max	Units
V_{CCO}		2.375	2.5	2.625	V
Output High Voltage for Q and $\overline{Q}$	R_T = 100 Ω across Q and $\overline{Q}$ signals	1.25	1.425	1.6	V
Output Low Voltage for Q and $\overline{Q}$	R_T = 100 Ω across Q and $\overline{Q}$ signals	0.9	1.075	1.25	V
Differential Output Voltage (Q - $\overline{Q}$), Q = High (($\overline{Q}$ - Q), $\overline{Q}$ = High	R_T = 100 Ω across Q and $\overline{Q}$ signals	250	350	450	mV
Output Common-Mode Voltage	R_T = 100 Ω across Q and $\overline{Q}$ signals	1.125	1.25	1.375	V
Differential Input Voltage (Q - $\overline{Q}$), Q = High (($\overline{Q}$ - Q), $\overline{Q}$ = High	Common-mode input voltage = 1.25 V	100	350	NA	mV
Input Common-Mode Voltage	Differential input voltage = ±350 mV	0.2	1.25	2.2	V

LVPECL DC Specifications

These values are valid when driving a 100 Ω differential load only, i.e., a 100 Ω resistor between the two receiver pins. The V_{OH} levels are 200 mV below standard LVPECL levels and are compatible with devices tolerant of lower common-mode ranges. The following table summarizes the DC output specifications of LVPECL.

DC Parameter	Min	Max	Min	Max	Min	Max	Units
V_{CCO}	3.0		3.3		3.6		V
V_{OH}	1.8	2.11	1.92	2.28	2.13	2.41	V
V_{OL}	0.96	1.27	1.06	1.43	1.30	1.57	V
V_{IH}	1.49	2.72	1.49	2.72	1.49	2.72	V
V_{IL}	0.86	2.125	0.86	2.125	0.86	2.125	V
Differential Input Voltage	0.3	-	0.3	-	0.3	-	V

Virtex-E Switching Characteristics

Testing of switching parameters is modeled after testing methods specified by MIL-M-38510/605. All devices are 100% functionally tested. Internal timing parameters are derived from measuring internal test patterns. Listed below are representative values. For more specific, more precise, and worst-case guaranteed data, use the values reported by the static timing analyzer (TRCE in the Xilinx Development System) and back-annotated to the simulation net list. All timing parameters assume worst-case operating conditions (supply voltage and junction temperature). Values apply to all Virtex-E devices unless otherwise noted.

IOB Input Switching Characteristics

Input delays associated with the pad are specified for LVTTL levels. For other standards, adjust the delays with the values shown in "IOB Input Switching Characteristics Standard Adjustments" on page 5.

			Speed Grade			
Description	**Device**	**Symbol**	**-8**	**-7**	**-6**	**Units**
Propagation Delays						
Pad to I output, no delay	All	T_{IOPI}		0.8	0.8	ns, max
Pad to I output, with delay	XCV50E	T_{IOPID}		1.0	1.0	ns, max
	XCV100E			1.0	1.0	ns, max
	XCV200E			1.0	1.0	ns, max
	XCV300E			1.0	1.0	ns, max
	XCV400E			1.0	1.0	ns, max
	XCV600E			1.0	1.0	ns, max
	XCV1000E			1.1	1.1	ns, max
	XCV1600E			1.1	1.1	ns, max
	XCV2000E			1.1	1.1	ns, max
Pad to output IQ via transparent latch, no delay	All	T_{IOPLI}		1.5	1.6	ns, max
Pad to output IQ via transparent latch, with delay	XCV50E	T_{IOPLID}		3.0	3.1	ns, max
	XCV100E			3.0	3.1	ns, max
	XCV200E			3.2	3.3	ns, max
	XCV300E			3.2	3.3	ns, max
	XCV400E			3.3	3.4	ns, max
	XCV600E			3.6	3.7	ns, max
	XCV1000E			3.6	3.7	ns, max
	XCV1600E			3.7	3.8	ns, max
	XCV2000E			3.7	3.8	ns, max
Sequential Delays						
Clock CLK to output IQ	All	T_{IOCKIQ}		0.7	0.7	ns, max
Setup and Hold Times with respect to Clock at IOB Input Register						
Pad, no delay	All	T_{IOPICK}/T_{IOICKP}		1.4 / 0	1.5 / 0	ns, min
Pad, with delay	All	$T_{IOPICKD}/T_{IOICKPD}$		3.1 / 0	3.1 / 0	ns, min
ICE input	All	$T_{IOICECK}/T_{IOCKICE}$		0.7 / 0	0.7 / 0	ns, min
SR input (IFF, synchronous)	All	$T_{IOSRCKI}$		0.9	1.0	ns, min
Set/Reset Delays						
SR input to IQ (asynchronous)	All	T_{IOSRIQ}		1.2	1.4	ns, max
GSR to output IQ	All	T_{GSRQ}		8.5	9.7	ns, max

Note: A Zero "0" Hold Time listing indicates no hold time or a negative hold time. Negative values can not be guaranteed "best-case", but if a "0" is listed, there is no positive hold time.

IOB Input Switching Characteristics Standard Adjustments

			Speed Grade			
Description	**Symbol**	**Standard**	**-8**	**-7**	**-6**	**Units**
Data Input Delay Adjustments						
Standard-specific data input delay adjustments	T_{ILVTTL}	LVTTL		0.0	0.0	ns
	$T_{ILVCMOS2}$	LVCMOS2		0.0	0.0	ns
	$T_{ILVCMOS18}$	LVCMOS18		0.20	0.20	ns
	T_{ILVDS}	LVDS		0.15	0.15	ns
	$T_{ILVPECL}$	LVPECL		0.15	0.15	ns
	T_{IPCI33_3}	PCI, 33 MHz, 3.3 V		0.08	0.08	ns
	T_{IPCI66_3}	PCI, 66 MHz, 3.3 V		0.0	0.0	ns
	T_{IGTL}	GTL		0.14	0.14	ns
	$T_{IGTLPLUS}$	GTL+		0.14	0.14	ns
	T_{IHSTL}	HSTL		0.04	0.04	ns
	T_{IHSTL2}	SSTL2		0.04	0.04	ns
	T_{IHSTL3}	SSTL3		0.04	0.04	ns
	T_{ICTTL}	CTT		0.10	0.10	ns
	T_{IAGP}	AGP		0.04	0.04	ns

IOB Output Switching Characteristics

Output delays terminating at a pad are specified for LVTTL with 12 mA drive and fast slew rate. For other standards, adjust the delays with the values shown in "IOB Output Switching Characteristics Standard Adjustments" on page 7.

		Speed Grade			
Description	**Symbol**	**-8**	**-7**	**-6**	**Units**
Propagation Delays					
O input to Pad	T_{IOOP}		2.7	2.9	ns, max
O input to Pad via transparent latch	T_{IOOLP}		3.1	3.4	ns, max
3-State Delays					
T input to Pad high-impedance (Note 1)	T_{IOTHZ}		1.7	1.9	ns, max
T input to valid data on Pad	T_{IOTON}		2.9	3.1	ns, max
T input to Pad high-impedance via transparent latch (Note 1)	$T_{IOTLPHZ}$		2.0	2.2	ns, max
T input to valid data on Pad via transparent latch	$T_{IOTLPON}$		3.2	3.4	ns, max
GTS to Pad high impedance (Note 1)	T_{GTS}		4.6	4.9	ns, max
Sequential Delays					
Clock CLK to Pad	T_{IOCKP}		2.8	2.9	ns, max
Clock CLK to Pad high-impedance (synchronous) (Note 1)	T_{IOCKHZ}		2.0	2.2	ns, max
Clock CLK to valid data on Pad (synchronous)	T_{IOCKON}		3.2	3.4	ns, max
Setup and Hold Times before/after Clock CLK					
O input	T_{IOOCK}/T_{IOCKO}		1.0 / 0	1.1 / 0	ns, min
OCE input	$T_{IOOCECK}/T_{IOCKOCE}$		0.7 / 0	0.7 / 0	ns, min
SR input (OFF)	$T_{IOSRCKO}/T_{IOSRCKO}$		1.0 / 0	1.1 / 0	ns, min
3-State Setup Times, T input	T_{IOTCK}/T_{IOCKT}		0.6 / 0	0.7 / 0	ns, min
3-State Setup Times, TCE input	$T_{IOTCECK}/T_{IOCKTCE}$		0.7 / 0	0.8 / 0	ns, min
3-State Setup Times, SR input (TFF)	$T_{IOSRCKT}/T_{IOCKTSR}$		0.9 / 0	1.0 / 0	ns, min
Set/Reset Delays					
SR input to Pad (asynchronous)	T_{IOSRP}		3.3	3.5	ns, max
SR input to Pad high-impedance (asynchronous) (Note 1)	T_{IOSRHZ}		2.4	2.7	ns, max
SR input to valid data on Pad (asynchronous)	T_{IOSRON}		3.7	3.9	ns, max
GSR to Pad	T_{IOGSRQ}		8.5	9.7	ns, max

Note: A Zero "0" Hold Time listing indicates no hold time or a negative hold time. Negative values can not be guaranteed "best-case", but if a "0" is listed, there is no positive hold time.
Note 1: Tri-state turn-off delays should not be adjusted.

IOB Output Switching Characteristics Standard Adjustments

Output delays terminating at a pad are specified for LVTTL with 12 mA drive and fast slew rate. For other standards, adjust the delays by the values shown.

			Speed Grade			
Description	**Symbol**	**Standard**	**-8**	**-7**	**-6**	**Units**
Output Delay Adjustments						
Standard-specific adjustments for output delays terminating at pads (based on standard capacitive load, Csl)	T_{OLVTTL_S2}	LVTTL, Slow,2 mA		14.7	14.7	ns
	T_{OLVTTL_S4}	4 mA		7.5	7.5	ns
	T_{OLVTTL_S6}	6 mA		4.8	4.8	ns
	T_{OLVTTL_S8}	8 mA		3.0	3.0	ns
	T_{OLVTTL_S12}	12 mA		1.9	1.9	ns
	T_{OLVTTL_S16}	16 mA		1.7	1.7	ns
	T_{OLVTTL_S24}	24 mA		1.3	1.3	ns
	T_{OLVTTL_F2}	LVTTL, Fast,2 mA		13.1	13.1	ns
	T_{OLVTTL_F4}	4 mA		5.3	5.3	ns
	T_{OLVTTL_F6}	6 mA		3.1	3.1	ns
	T_{OLVTTL_F8}	8 mA		1.0	1.0	ns
	T_{OLVTTL_F12}	12 mA		0.0	0.0	ns
	T_{OLVTTL_F16}	16 mA		-0.05	-0.05	ns
	T_{OLVTTL_F24}	24 mA		-0.20	-0.20	ns
	$T_{OLVCMOS\_2}$	LVCMOS2		0.09	0.09	ns
	$T_{OLVCMOS\_18}$	LVCMOS18		0.7	0.7	ns
	T_{OLVDS}	LVDS		-1.2	-1.2	ns
	$T_{OLVPECL}$	LVPECL		-0.41	-0.41	ns
	$T_{OPCI\_33\_3}$	PCI, 33 MHz, 3.3 V		2.3	2.3	ns
	$T_{OPCI\_66\_3}$	PCI, 66 MHz, 3.3 V		-0.41	-0.41	ns
	T_{OGTL}	GTL		0.49	0.49	ns
	T_{OGTLP}	GTL+		0.8	0.8	ns
	T_{OHSTL_I}	HSTL I		-0.51	-0.51	ns
	T_{OHSTL_IIII}	HSTL III		-0.9	-0.9	ns
	T_{OHSTL_IV}	HSTL IV		-1.0	-1.0	ns
	T_{OSSTL2_I}	SSTL2 I		-0.51	-0.51	ns
	T_{OSSTL2_II}	SSTL2 II		-1.0	-1.0	ns
	T_{OSSTL3_I}	SSTL3 I		-0.51	-0.51	ns
	T_{OSSTL3_II}	SSTL3 II		-0.9	-0.9	ns
	T_{OCTT}	CTT		-0.6	-0.6	ns
	T_{OAGP}	AGP		-0.9	-0.9	ns

Calculation of T_{ioop} as a Function of Capacitance

The values for T_{ioop} were based on the standard capacitive load (Csl) for each IO standard as listed in Table 1.

For other capacitive loads, use the formulas below to calculate the corresponding T_{ioop}.

$$T_{ioop} = T_{ioop} + T_{opadjust} + (C_{load} - C_{sl}) * fl$$

Where:

$T_{opadjust}$ is reported above in the Output Delay Adjustment section.
C_{load} is the capacitive load for the design.

Table 1: Constants for Use in Calculation of T_{ioop}

Standard	Csl (pF)	fl (ns/pF)
LVTTL Fast Slew Rate, 2mA drive	35	0.41
LVTTL Fast Slew Rate, 4mA drive	35	0.20
LVTTL Fast Slew Rate, 6mA drive	35	0.13
LVTTL Fast Slew Rate, 8mA drive	35	0.079
LVTTL Fast Slew Rate, 12mA drive	35	0.044
LVTTL Fast Slew Rate, 16mA drive	35	0.043
LVTTL Fast Slew Rate, 24mA drive	35	0.033
LVTTL Slow Slew Rate, 2mA drive	35	0.41
LVTTL Slow Slew Rate, 4mA drive	35	0.20
LVTTL Slow Slew Rate, 6mA drive	35	0.10
LVTTL Slow Slew Rate, 8mA drive	35	0.086
LVTTL Slow Slew Rate, 12mA drive	35	0.058
LVTTL Slow Slew Rate, 16mA drive	35	0.050
LVTTL Slow Slew Rate, 24mA drive	35	0.048
LVCMOS2	35	0.041
LVCMOS18	35	0.050
PCI 33MHZ 3.3 V	10	0.050
PCI 66 MHz 3.3 V	10	0.033
GTL	0	0.014
GTL+	0	0.017
HSTL Class I	20	0.022
HSTL Class III	20	0.016
HSTL Class IV	20	0.014
SSTL2 Class I	30	0.028
SSTL2 Class II	30	0.016
SSTL3 Class I	30	0.029
SSTL3 Class II	30	0.016
CTT	20	0.035
AGP	10	0.037

Clock Distribution Switching Characteristics

		Speed Grade			
Description	**Symbol**	**-8**	**-7**	**-6**	**Units**
GCLK IOB and Buffer					
Global Clock PAD to output.	T_{GPIO}		0.7	0.7	ns, max
Global Clock Buffer I input to O output	T_{GIO}		0.7	0.7	ns, max

CLB Switching Characteristics

Delays originating at F/G inputs vary slightly according to the input used. The values listed below are worst-case. Precise values are provided by the timing analyzer.

		Speed Grade			
Description	**Symbol**	**-8**	**-7**	**-6**	**Units**
Combinatorial Delays					
4-input function: F/G inputs to X/Y outputs	T_{ILO}		0.5	0.5	ns, max
5-input function: F/G inputs to F5 output	T_{IF5}		0.8	0.9	ns, max
5-input function: F/G inputs to X output	T_{IF5X}		0.8	0.9	ns, max
6-input function: F/G inputs to Y output via F6 MUX	T_{IF6Y}		0.9	1.0	ns, max
6-input function: F5IN input to Y output	T_{F5INY}		0.2	0.2	ns, max
Incremental delay routing through transparent latch to XQ/YQ outputs	T_{IFNCTL}		0.6	0.7	ns, max
BY input to YB output	T_{BYYB}		0.5	0.6	ns, max
Sequential Delays					
FF Clock CLK to XQ/YQ outputs	T_{CKO}		0.9	1.0	ns, max
Latch Clock CLK to XQ/YQ outputs	T_{CKLO}		0.9	1.0	ns, max
Setup and Hold Times before/after Clock CLK					
4-input function: F/G Inputs	T_{ICK}/T_{ICK}		0.9 / 0	1.0 / 0	ns, min
5-input function: F/G inputs	T_{IF5CK}/T_{CKIF5}		1.3 / 0	1.5 / 0	ns, min
6-input function: F5IN input	T_{F5INCK}/T_{CKF5IN}		0.7 / 0	0.8 / 0	ns, min
6-input function: F/G inputs via F6 MUX	T_{IF6CK}/T_{CKIF6}		1.5 / 0	1.6 / 0	ns, min
BX/BY inputs	T_{DICK}/T_{CKDI}		0.6 / 0	0.7 / 0	ns, min
CE input	T_{CECK}/T_{CKCE}		0.7 / 0	0.7 / 0	ns, min
SR/BY inputs (synchronous)	T_{RCK}/T_{CKR}		0.6 / 0	0.7 / 0	ns, min
Clock CLK					
Minimum Pulse Width, High	T_{CH}		1.3	1.4	ns, min
Minimum Pulse Width, Low	T_{CL}		1.3	1.4	ns, min
Set/Reset					
Minimum Pulse Width, SR/BY inputs	T_{RPW}		2.1	2.4	ns, min
Delay from SR/BY inputs to XQ/YQ outputs (asynchronous)	T_{RQ}		0.9	1.0	ns, max
Toggle Frequency (MHz) (for export control)	F_{TOG}		384	357	MHz

Note: A Zero “0” Hold Time listing indicates no hold time or a negative hold time. Negative values can not be guaranteed “best-case”, but if a “0” is listed, there is no positive hold time.

CLB Arithmetic Switching Characteristics

Setup times not listed explicitly can be approximated by decreasing the combinatorial delays by the setup time adjustment listed. Precise values are provided by the timing analyzer.

		Speed Grade			
Description	**Symbol**	**-8**	**-7**	**-6**	**Units**
Combinatorial Delays					
F operand inputs to X via XOR	T_{OPX}		0.8	0.8	ns, max
F operand input to XB output	T_{OPXB}		0.8	0.9	ns, max
F operand input to Y via XOR	T_{OPY}		1.4	1.5	ns, max
F operand input to YB output	T_{OPYB}		1.3	1.4	ns, max
F operand input to COUT output	T_{OPCYF}		1.0	1.1	ns, max
G operand inputs to Y via XOR	T_{OPGY}		0.8	0.9	ns, max
G operand input to YB output	T_{OPGYB}		1.3	1.5	ns, max
G operand input to COUT output	T_{OPCYG}		1.0	1.1	ns, max
BX initialization input to COUT	T_{BXCY}		0.5	0.6	ns, max
CIN input to X output via XOR	T_{CINX}		0.6	0.7	ns, max
CIN input to XB	T_{CINXB}		0.07	0.08	ns, max
CIN input to Y via XOR	T_{CINY}		0.7	0.7	ns, max
CIN input to YB	T_{CINYB}		0.4	0.4	ns, max
CIN input to COUT output	T_{BYP}		0.1	0.2	ns, max
Multiplier Operation					
F1/2 operand inputs to XB output via AND	T_{FANDXB}		0.3	0.3	ns, max
F1/2 operand inputs to YB output via AND	T_{FANDYB}		0.8	0.9	ns, max
F1/2 operand inputs to COUT output via AND	T_{FANDCY}		0.5	0.6	ns, max
G1/2 operand inputs to YB output via AND	T_{GANDYB}		0.5	0.5	ns, max
G1/2 operand inputs to COUT output via AND	T_{GANDCY}		0.2	0.3	ns, max
Setup and Hold Times before/after Clock CLK					
CIN input to FFX	T_{CCKX}/T_{CKCX}		1.1 / 0	1.2 / 0	ns, min
CIN input to FFY	T_{CCKY}/T_{CKCY}		1.2 / 0	1.3 / 0	ns, min

Note: A Zero “0” Hold Time listing indicates no hold time or a negative hold time. Negative values can not be guaranteed “best-case”, but if a “0” is listed, there is no positive hold time.

CLB SelectRAM Switching Characteristics

Description	Symbol	Speed Grade			Units
		-8	-7	-6	
Sequential Delays					
Clock CLK to X/Y outputs (WE active)	T_{SHCKO}		1.7	1.9	ns, max
Shift-Register Mode Clock CLK to X/Y outputs			1.7	1.9	ns, max
Setup and Hold Times before/after Clock CLK					
F/G address inputs	T_{AS}/T_{AH}		0.5 / 0	0.5 / 0	ns, min
BX/BY data inputs (DIN)	T_{DS}/T_{DH}		0.6 / 0	0.6 / 0	ns, min
CE input (WE)	T_{WS}/T_{WH}		0.7 / 0	0.8 / 0	ns, min
Shift-Register Mode BX/BY data inputs (DIN) CE input (WS)	 T_{SHDICK} T_{SHCECK}		 0.6 / 0 0.7 / 0	 0.6 / 0 0.8 / 0	 ns, min ns, min
Clock CLK					
Minimum Pulse Width, High	T_{WPH}		2.1	2.4	ns, min
Minimum Pulse Width, Low	T_{WPL}		2.1	2.4	ns, min
Minimum clock period to meet address write cycle time	T_{WC}		4.2	4.8	ns, min
Shift-Register Mode Minimum Pulse Width, High Minimum Pulse Width, Low	 T_{SRPH} T_{SRPL}		 2.1 2.1	 2.4 2.4	 ns, min ns, min

Note: A Zero “0” Hold Time listing indicates no hold time or a negative hold time. Negative values can not be guaranteed “best-case”, but if a “0” is listed, there is no positive hold time.

BlockRAM Switching Characteristics

Description	Symbol	Speed Grade			Units
		-8	-7	-6	
Sequential Delays					
Clock CLK to DOUT output	T_{BCKO}		2.6	2.9	ns, max
Setup and Hold Times before Clock CLK					
ADDR inputs	T_{BACK}/T_{BACK}		1.0 / 0	1.1 / 0	ns, min
DIN inputs	T_{BDCK}/T_{BCKD}		1.0 / 0	1.1 / 0	ns, min
EN input	T_{BECK}/T_{BCKE}		2.2 / 0	2.5 / 0	ns, min
RST input	T_{BRCK}/T_{BCKR}		2.1 / 0	2.3 / 0	ns, min
WEN input	T_{BWCK}/T_{BCKW}		2.0 / 0	2.2 / 0	ns, min
Clock CLK					
Minimum Pulse Width, High	T_{BPWH}		1.4	1.5	ns, min
Minimum Pulse Width, Low	T_{BPWL}		1.4	1.5	ns, min

Note: A Zero “0” Hold Time listing indicates no hold time or a negative hold time. Negative values can not be guaranteed “best-case”, but if a “0” is listed, there is no positive hold time.

TBUF Switching Characteristics

Description	Symbol	Speed Grade			Units
		-8	-7	-6	
Combinatorial Delays					
IN input to OUT output	T_{IO}		0	0	ns, max
TRI input to OUT output high-impedance	T_{OFF}		0.10	0.11	ns, max
TRI input to valid data on OUT output	T_{ON}		0.10	0.11	ns, max

JTAG Test Access Port Switching Characteristics

Description	Symbol	Speed Grade			Units
		-8	-7	-6	
TMS and TDI Setup times before TCK	T_{TAPTK}			4.0	ns, min
TMS and TDI Hold times after TCK	T_{TCKTAP}			2.0	ns, min
Output delay from clock TCK to output TDO	T_{TCKTDO}			11.0	ns, max
Maximum TCK clock frequency	F_{TCK}			33	MHz, max

Virtex-E Pin-to-Pin Output Parameter Guidelines

Testing of switching parameters is modeled after testing methods specified by MIL-M-38510/605. All devices are 100% functionally tested. Listed below are representative values for typical pin locations and normal clock loading. Values are expressed in nanoseconds unless otherwise noted.

Global Clock Input to Output Delay for LVTTL, 12 mA, Fast Slew Rate, *with* DLL

		Speed Grade	-8	-7	-6	Units
Description	**Symbol**	**Device**	**Max**	**Max**	**Max**	
LVTTL Global Clock Input to Output Delay using Output Flip-flop, 12 mA, Fast Slew Rate, *with* DLL. For data *output* with different standards, adjust the delays with the values shown in "IOB Output Switching Characteristics Standard Adjustments" on page 7.	$T_{ICKOFDLL}$	XCV50E		3.1	3.1	ns
		XCV100E		3.1	3.1	ns
		XCV200E		3.1	3.1	ns
		XCV300E		3.1	3.1	ns
		XCV400E		3.1	3.1	ns
		XCV600E		3.1	3.1	ns
		XCV1000E		3.1	3.1	ns
		XCV1600E		3.1	3.1	ns
		XCV2000E		3.1	3.1	ns

Notes: Listed above are representative values where one global clock input drives one vertical clock line in each accessible column, and where all accessible IOB and CLB flip-flops are clocked by the global clock net.
Output timing is measured at 50% V_{CC} threshold with 35 pF external capacitive load. For different loads, see Table 1.
DLL output jitter is already included in the timing calculation.

Global Clock Input to Output Delay for LVTTL, 12 mA, Fast Slew Rate, *without* DLL

		Speed Grade	-8	-7	-6	Units
Description	**Symbol**	**Device**	**Max**	**Max**	**Max**	
LVTTL Global Clock Input to Output Delay using Output Flip-flop, 12 mA, Fast Slew Rate, *without* DLL. For data *output* with different standards, adjust the delays with the values shown in "IOB Output Switching Characteristics Standard Adjustments" on page 7.	T_{ICKOF}	XCV50E		4.4	4.6	ns
		XCV100E		4.4	4.6	ns
		XCV200E		4.5	4.7	ns
		XCV300E		4.5	4.7	ns
		XCV400E		4.6	4.8	ns
		XCV600E		4.7	4.9	ns
		XCV1000E		4.8	5.0	ns
		XCV1600E		4.9	5.1	ns
		XCV2000E		5.0	5.2	ns

Notes: Listed above are representative values where one global clock input drives one vertical clock line in each accessible column, and where all accessible IOB and CLB flip-flops are clocked by the global clock net.
Output timing is measured at 50% V_{CC} threshold with 35 pF external capacitive load. For different loads, see Table 1.

Virtex-E Pin-to-Pin Input Parameter Guidelines

Testing of switching parameters is modeled after testing methods specified by MIL-M-38510/605. All devices are 100% functionally tested. Listed below are representative values for typical pin locations and normal clock loading. Values are expressed in nanoseconds unless otherwise noted

Global Clock Set-Up and Hold for LVTTL Standard, *with* DLL

		Speed Grade	-8	-7	-6	Units
Description	**Symbol**	**Device**	**Min**	**Min**	**Min**	
Input Setup and Hold Time Relative to Global Clock Input Signal for LVTTL Standard. For data input with different standards, adjust the setup time delay by the values shown in "IOB Input Switching Characteristics Standard Adjustments" on page 5.						
No Delay	T_{PSDLL}/T_{PHDLL}	XCV50E		1.5 / -0.4	1.5 / -0.4	ns
Global Clock and IFF, with DLL		XCV100E		1.5 / -0.4	1.5 / -0.4	ns
		XCV200E		1.5 / -0.4	1.5 / -0.4	ns
		XCV300E		1.5 / -0.4	1.5 / -0.4	ns
		XCV400E		1.5 / -0.4	1.5 / -0.4	ns
		XCV600E		1.5 / -0.4	1.5 / -0.4	ns
		XCV1000E		1.5 / -0.4	1.5 / -0.4	ns
		XCV1600E		1.5 / -0.4	1.5 / -0.4	ns
		XCV2000E		1.5 / -0.4	1.5 / -0.4	ns

IFF = Input Flip-Flop or Latch

Notes: Setup time is measured relative to the Global Clock input signal with the fastest route and the lightest load. Hold time is measured relative to the Global Clock input signal with the slowest route and heaviest load.

DLL output jitter is already included in the timing calculation.

Global Clock Set-Up and Hold for LVTTL Standard, *without* DLL

		Speed Grade	-8	-7	-6	Units
Description	**Symbol**	**Device**	**Min**	**Min**	**Min**	
Input Setup and Hold Time Relative to Global Clock Input Signal for LVTTL Standard. For data input with different standards, adjust the setup time delay by the values shown in "IOB Input Switching Characteristics Standard Adjustments" on page 5.						
Full Delay	T_{PSFD}/T_{PHFD}	XCV50E		2.3 / 0	2.3 / 0	ns
Global Clock and IFF, without DLL		XCV100E		2.3 / 0	2.3 / 0	ns
		XCV200E		2.4 / 0	2.4 / 0	ns
		XCV300E		2.5 / 0	2.5 / 0	ns
		XCV400E		2.5 / 0	2.5 / 0	ns
		XCV600E		2.6 / 0	2.6 / 0	ns
		XCV1000E		2.8 / 0	2.8 / 0	ns
		XCV1600E		3.0 / 0	3.0 / 0	ns
		XCV2000E		3.2 / 0	3.2 / 0	ns

IFF = Input Flip-Flop or Latch

Note: Setup time is measured relative to the Global Clock input signal with the fastest route and the lightest load. Hold time is measured relative to the Global Clock input signal with the slowest route and heaviest load.

A Zero "0" Hold Time listing indicates no hold time or a negative hold time. Negative values can not be guaranteed "best-case", but if a "0" is listed, there is no positive hold time.

DLL Timing Parameters

Switching parameters testing is modeled after testing methods specified by MIL-M-38510/605; all devices are 100 percent functionally tested. Because of the difficulty in directly measuring many internal timing parameters, those parameters are derived from benchmark timing patterns. The following guidelines reflect worst-case values across the recommended operating conditions.

		Speed Grade	-8		-7		-6		
Description	**Symbol**	**F_{CLKIN}**	**Min**	**Max**	**Min**	**Max**	**Min**	**Max**	**Units**
Input Clock Frequency (CLKDLLHF)	$F_{CLKINHF}$				60	320	60	260	MHz
Input Clock Frequency (CLKDLL)	$F_{CLKINLF}$				25	160	25	130	MHz
Input Clock Low/High Pulse Width	T_{DLLPW}	≥25 MHz			5.0		5.0		ns
		≥50 MHz			3.0		3.0		ns
		≥100 MHz			2.4		2.4		ns
		≥150 MHz			2.0		2.0		ns
		≥200 MHz			1.8		1.8		ns
		≥250 MHz			1.5		1.5		ns
		≥300 MHz			1.3		NA		ns

Note: All specifications correspond to Commercial Operating Temperatures (0˚C to +85˚C).

DLL Clock Tolerance, Jitter, and Phase Information

All DLL output jitter and phase specifications determined through statistical measurement at the package pins using a clock mirror configuration and matched drivers.

			CLKDLLHF		CLKDLL		
Description	**Symbol**	**F_{CLKIN}**	**Min**	**Max**	**Min**	**Max**	**Units**
Input Clock Period Tolerance	T_{IPTOL}		-	1.0	-	1.0	ns
Input Clock Jitter Tolerance (Cycle to Cycle)	T_{IJITCC}		-	± 150	-	± 300	ps
Time Required for DLL to Acquire Lock	T_{LOCK}	> 60 MHz	-	20	-	20	µs
		50 - 60 MHz	-	-	-	25	µs
		40 - 50 MHz	-	-	-	50	µs
		30 - 40 MHz	-	-	-	90	µs
		25 - 30 MHz	-	-	-	120	µs
Output Jitter (cycle-to-cycle) for any DLL Clock Output[1]	T_{OJITCC}			± 60		± 60	ps
Phase Offset between CLKIN and CLKO[2]	T_{PHIO}			± 100		± 100	ps
Phase Offset between any DLL Clock Outputs[3]	T_{PHOO}			± 140		± 140	ps
Maximum Phase Difference between CLKIN and CLKO[4]	T_{PHIOM}			± 160		± 160	ps
Maximum Phase Difference between any DLL Clock Outputs[5]	T_{PHOOM}			± 200		± 200	ps

Note 1: **Output Jitter** is cycle-to-cycle jitter measured on the DLL output clock, *excluding* input clock jitter.
Note 2: **Phase Offset between CLKIN and CLKO** is the worst-case fixed time difference between rising edges of CLKIN and CLKO, *excluding* Output Jitter and input clock jitter.
Note 3: **Phase Offset between any DLL Clock Outputs** is the worst-case fixed time difference between rising edges of any two DLL outputs, *excluding* Output Jitter and input clock jitter.
Note 4: **Maximum Phase Difference between CLKIN an CLKO** is the sum of Output Jitter and Phase Offset between CLKIN and CLKO, or the greatest difference between CLKIN and CLKO rising edges due to DLL alone (*excluding* input clock jitter).
Note 5: **Maximum Phase DIfference between any DLL Clock Outputs** is the sum of Output JItter and Phase Offset between any DLL clock outputs, or the greatest difference between any two DLL output rising edges sue to DLL alone (*excluding* input clock jitter).
Note 6: All specifications correspond to Commercial Operating Temperatures (0˚C to +85˚C).

Period Tolerance: the allowed input clock period change.

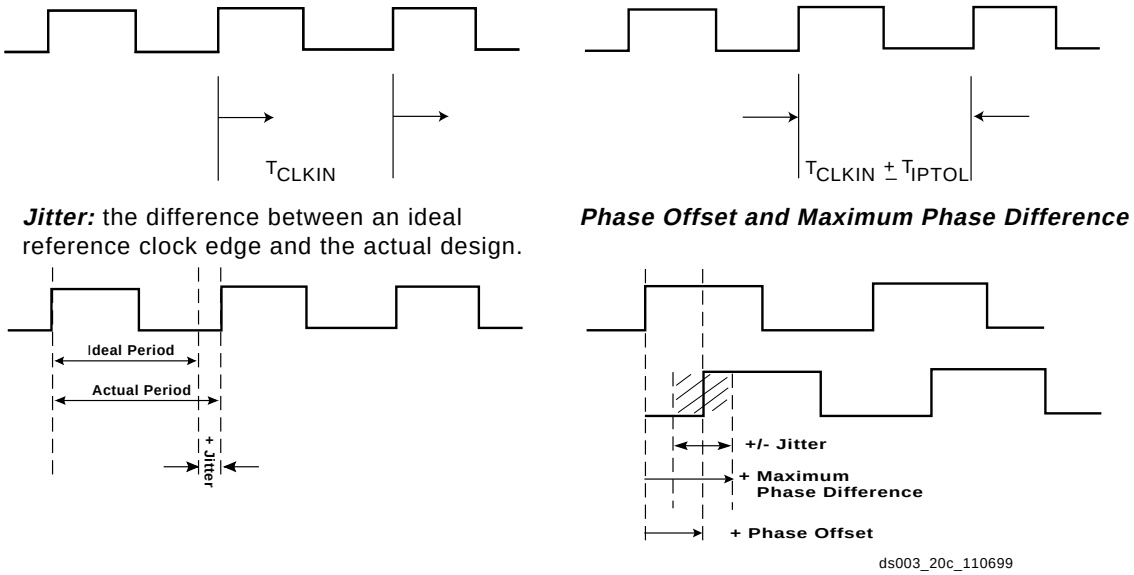

Figure 1: DLL Timing Waveforms

Revision History

Version	Description
1.0 (12/2/99)	Initial Release