Configuring Mixed FPGA Daisy Chains

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Overview

Xilinx FPGAs can be configured in a common daisy-chain structure, where the lead device generates CCLK pulses and feeds serial configuration information into the next downstream device, which in turn feeds data into the next downstream device, etc. There is no limit to the number of devices in a daisy chain, and XC2000, XC3000, XC4000, and XC5200 series devices can be mixed freely with only one constraint: the lead device must be a member of the highest-order family used in the chain. (For the purposes of this discussion, there is no difference between the XC4000 series and the XC5200 family, when XC5200 is used in any configuration mode except Express Mode). The lead device must generate a sufficient number of CCLK pulses after length-count-match was achieved, but XC3000-series devices generate fewer CCLK pulses than XC4000-series or XC5200-family devices require, and XC2000 devices generate even fewer CCLK pulses after length-count match. See Figure 1.

In a daisy-chain, all CCLK pins are interconnected, and DOUT of any upstream device feeds the DIN input of its downstream neighbor. Those are the basic connections. For control purposes, it is advisable to interconnect all the slave $\overline{\text{INIT}}$ pins (the XC2000 does not have this pin) and connect them to the $\overline{\text{INIT}}$ pin of the lead XC4000/XC5200 device or the $\overline{\text{RESET}}$ input of the lead XC3000 device.

Interconnected $\overline{\text{INIT}}$ pins prevent the master from starting the configuration process until all slaves are ready. For power-up this is assured automatically, since the master uses four times as many internal clocks for the power-up as any slave does, but, when re-configuring, master and slave devices consume the same number of clocks to clear a frame, and a fast master might be ready before a slow slave is. Interconnecting $\overline{\text{INIT}}$s solves this problem.

The DONE/$\overline{\text{PROG}}$ (D/$\overline{\text{P}}$) and $\overline{\text{RESET}}$ pins (XC2000, XC3000) and the XC4000/XC5200 $\overline{\text{PROGRAM}}$ pins can be used in different ways, depending on the designer's preferences regarding reconfiguration, pin utilization, and need for a global RESET input.

If there is no need for a global logic RESET input, then it is best to permanently ground the XC2000/3000 D/$\overline{\text{P}}$ pin, which means that the $\overline{\text{RESET}}$ input functions as the Reconfigure input, and should be connected to all XC4000/XC5200 *PROGRAM* inputs.

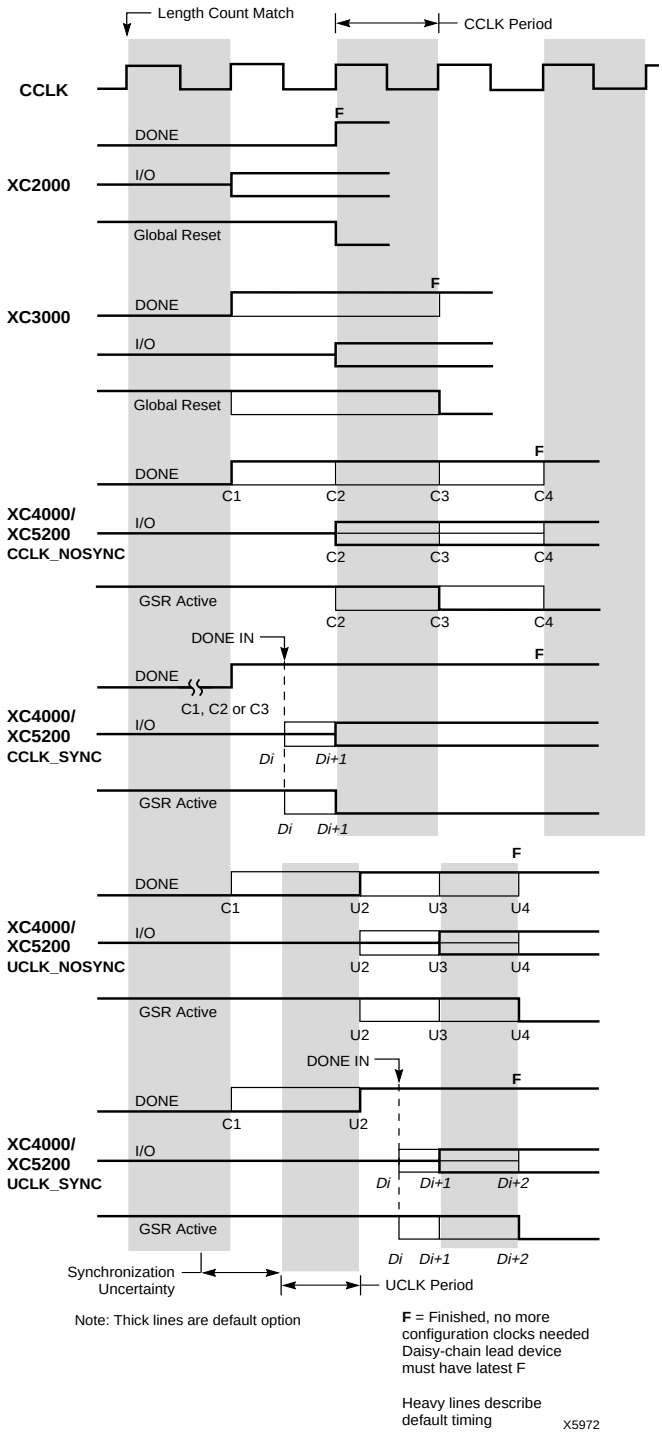

Figure 1: Start-up Timing

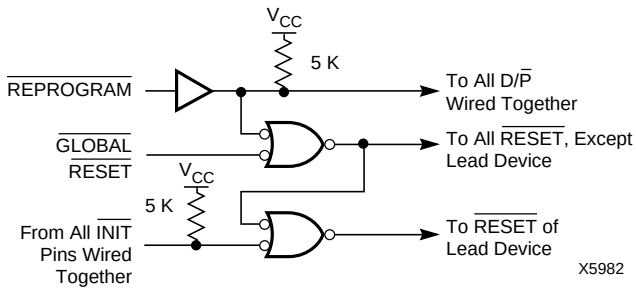

Figure 2:

If there is a need for a global logic RESET input that can reset all flip-flops in the user logic without causing reconfiguration, then external logic must combine RESET and D/P in such a way, that pulling Low RESET does not affect D/P, but pulling Low D/P also pulls down RESET. See Figure 2.

The following simple recommendations guarantee a well-defined beginning for any FPGA configuration or reconfiguration process, after the initialization and clearing of the configuration memory in all FPGAs has been completed, and the address counter in the serial PROM(s) has been reset.

The connections described below guarantee reliable operation even under adverse operating conditions such as V_{CC} glitches.

The lead device can use any configuration mode available. In all modes except Slave Serial, its CCLK pin is the output that clocks all other devices.

Obviously, all CCLK and XC1700 CLK pins must be interconnected, the DATA outputs from multiple XC1700 serial PROMs must be interconnected and connected to the DIN input of the lead device, and the daisy-chain must be established by connecting each DOUT output to the downstream DIN input.

Configuration control pins are:

XC3000A, XC3000L, XC3100, XC3100A:

DONE/PROGRAM (open-drain output/input)
RESET (input)
INIT (open-drain output)

XC4000 Series (XC4000E, XC4000X) and XC5200 family:

DONE (open-drain output / input)
PROGRAM (input)
INIT (open-drain output / input)

XC1700:

RESET (input with programmable polarity)

The following recommendations assume that there are no XC2000 devices in the daisy chain (they lack the INIT output) and that, if Serial mode is chosen for the lead device, the XC1700 device(s) store only one configuration for the whole daisy chain. The serial PROM(s) must, therefore, be reset before the daisy chain is to be (re)programmed.

There are three possible types of daisy chains using XC3000 and XC4000/XC5200 devices. Here are the recommended connections for the configuration control pins.

Case 1:
Daisy chain consists of nothing but XC3000-series devices:

Use lead device's LDC to drive XC1700 CE.

Use lead device's INIT to drive XC1700 RESET.

Interconnect all slave INITs and connect them to the lead *RESET* input.

Interconnect all DONE pins.

Interconnect all slave RESET inputs

Instigate Reprogram by pulling the slave RESET net Low for at least 6 µs while all DONE pins are Low.

(DONE can be permanently wired Low, but that sacrifices the use of RESET as a global reset of the user logic. If DONE is not wired Low, reprogram must pull DONE Low with an open-collector or open-drain driver).

Case 2:
Lead device is XC4000-series or XC5200 family, driving any mixture of XC3000, XC4000 and XC5200 devices:

Use lead device's LDC to drive XC1700 CE.

Use lead device's INIT to drive XC1700 RESET.

Interconnect all INIT pins.

Interconnect all DONE pins.

Interconnect all XC4000/XC5200 PROGRAM inputs.

Interconnect all XC3000 RESET inputs.

Combine these two nets into one PROGRAM/RESET net

Instigate Reprogram by pulling the combined PROGRAM/RESET Low.

Case 3:
Daisy chain consists of nothing but XC4000/ and XC5200-type devices:

Use lead device's LDC to drive XC1700 CE.

Use lead device's INIT to drive XC1700 RESET.

Interconnect all INIT pins.

Interconnect all DONE pins (only required for UCLK-SYNC option).

Interconnect all XC4000/XC5200 PROGRAM inputs.

Instigate Reprogram by pulling PROGRAM Low.