ALLIANCE
Series Software

XILINX®

Synthesis • MTI
Implementation Flow

Module Generators

DSP COREGen

LogiBLOX

Verilog & VHDL
Instantiation

.VEI
.VHI

State Diagram Editor

HDL Editor

Schematic Design Editor

VHDL Verilog

VHDL Verilog

XNF EDIF

VHDL Verilog

VHDL Verilog

.NGO XNF

Black Box Instantiation

Behavioral Simulation Models

Functional Simulation Flow

Timing Requirements

Timing Simulation Flow

Model Technology

MODELSIM

SIMULATOR

Xilinx IMPLEMENTATION Tools

VHDL Verilog

SDF

3rd Party Synthesis

COREGen

LogiBLOX

UNISIM

VITAL & Verilog

SIMPRIM

VITAL & Verilog

HDL Test Bench

BIT JEDEC

XNF EDIF

VHDL Verilog

w/ Timing Constraints

.NGO= Xilinx Binary Netlist

Reports

User Constraints File

Functional Simulation Flow

EG