# Adaptive Instrument Module - A Reconfigurable Processor for Spacecraft Applications

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## *Abstract*

A reconfigurable computer optimized for spacecraft instrument use called the Adaptive Instrument Module (AIM) is under development and scheduled for launch in November 2000 on the Australian Fedsat spacecraft. The advent of RAM-based FPGAs whose configuration can be changed at any time has enabled the development of a low cost reconfigurable computer for space use. Reconfigurable computers provide solutions to problems that are uniquely found in spacecraft applications, but difficulties in using RAM-based FPGAs in the space environment must be overcome. The development of the AIM will allow future satellite programs to avoid the large costs associated with new builds by reconfiguring standardized processing hardware.

## I. INTRODUCTION

The use of reconfigurable logic and processors for spacecraft applications provides numerous benefits. Design errors can be corrected after launch, higher performance can be achieved than with software based processing, and costs can be reduced by using common hardware designs. System performance can even be improved with updated hardware designs once on orbit performance is determined. This is particularly true for spacecraft instruments. However, the use of reconfigurable logic for spacecraft applications presents challenges not found in ground applications.

Electronics in space are adversely effected by radiation. Single event upsets (SEUs) due to energetic particles found in space can cause upsets or bit flips in memories. Reconfigurable logic based on SRAM-configured Field Programmable Gate Arrays (FPGAs) are particularly susceptible to these effects, since upsets can cause circuit operation to change, and not just cause a burst of invalid data. Fortunately, techniques can be developed to mitigate these effects. The use of reconfigurable processors in space must also address the limited resources on spacecraft.

This paper describes a reconfigurable processor called the Adaptive Instrument Module (AIM) that is optimized for space-based instruments. It is being developed for the Fedsat spacecraft and scheduled for launch in November 2000. It primarily addresses hardware design aspects of the AIM.

## II. SRAM-CONFIGURED FPGAS AS THE FOUNDATION OF A SPACECRAFT RECONFIGURABLE PROCESSOR

SRAM-configured FPGAs are programmed by loading a configuration bitstream into a device. The device functionality can be changed at anytime by loading in a new bitstream. This makes them ideal for use as the basis of a reconfigurable processor. In fact, several companies produce reconfigurable processor boards based on this type of FPGA for ground use. Such a reconfigurable processor implements algorithms directly in hardware and executes them up to orders of magnitude faster than a software implementation of the same algorithm. Possible algorithms include digital filters, image processing, and data compression. These algorithms can be specified using whatever design tools are available for the particular FPGA and may include the VHDL design language and schematic entry. In addition, many vendors sell Intellectual Property (IP) cores that implement useful algorithms.

The successful use of a reconfigurable processor on spacecraft must address several issues. First, provisions must be made to detect upsets in the configuration memory of the SRAM-configured FPGA, and reload the device with the correct configuration. Second, there must be a mechanism to store multiple configurations onboard, upload new configurations from the ground, and load configurations into the FPGA. The method of uploading new configurations must take into account the low data rate (1 Kbit per second or less) found on most spacecraft.

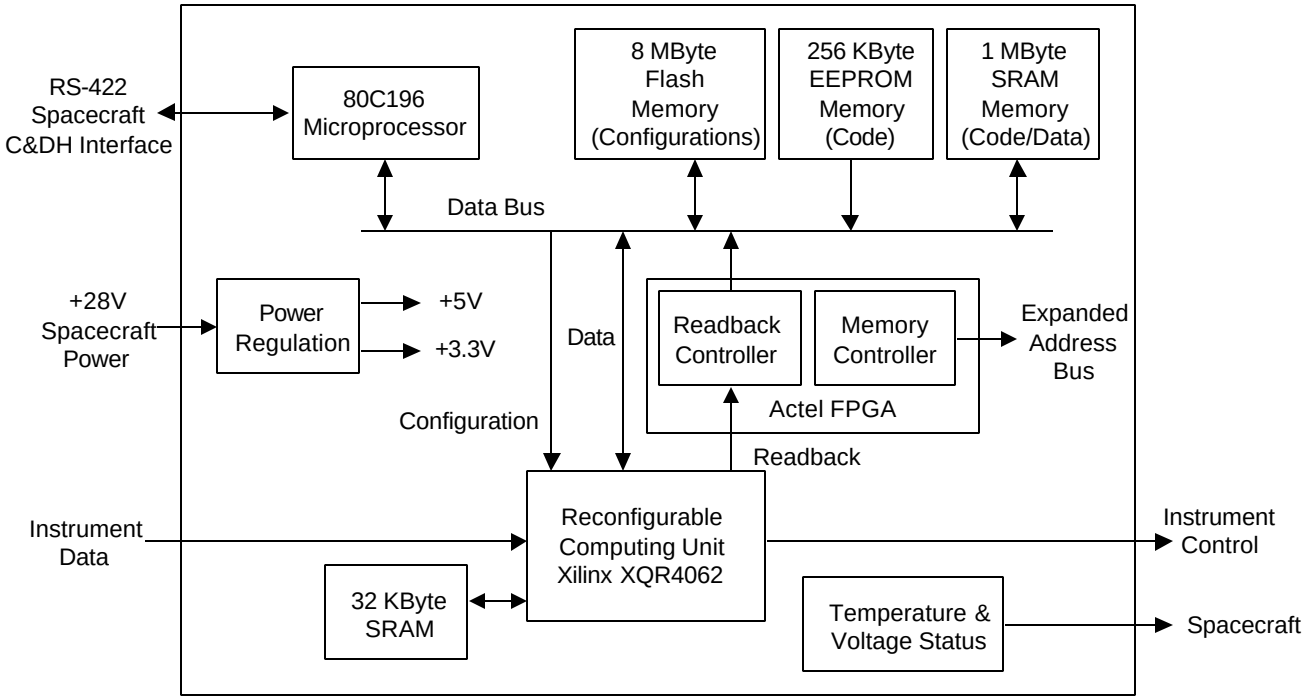


Figure 1 AIM Block Diagram

## III. Adaptive Instrument Module Design Requirements

Until a reconfigurable processor is successfully demonstrated in space, many spacecraft programs will not consider using one despite the advantages. An actual flight will demonstrate the feasibility of a space-based reconfigurable processor. Such an opportunity exists on the Australian Fedsat spacecraft that is scheduled for launch in November 2000. This is a university class spacecraft carrying several experiments. The Adaptive Instrument Module is one of the experiment payloads. The Johns Hopkins University Applied Physics Laboratory (JHU/APL) is teaming with the Queensland University of Technology (QUT) in designing the AIM for the Fedsat spacecraft. QUT, with its background in reconfigurable computing, is providing the system level requirements, software design, spacecraft integration of the AIM, and post-launch mission operations. JHU/APL, with its long history of flight electronics design and fabrication, is doing the hardware design and flight hardware fabrication of the AIM.

The design of the AIM takes into account a limited budget, parts availability, power and weight limitations, and program schedule. The top-level requirements of the AIM are:

- Use the Xilinx XQR4062 FPGA as the foundation of the reconfigurable processor
- Store and manage multiple Xilinx FPGA configurations
- Upload additional FPGA configurations
- Detect, correct, and log single event upset induced configuration errors autonomously in the Xilinx
- Run standalone reconfigurable computing experiments
- Process instrument data with reconfigurable hardware
- Interface to spacecraft command and data handling system
- Generate secondary voltages from the spacecraft +28V bus

The Xilinx XQR4062 was selected for use as the foundation of the reconfigurable processor because it is available in a radiation tolerant version that can survive for several years in typical spacecraft orbits. It also has sufficient resources (gates and memory cells) to implement algorithms of significant complexity for spacecraft instruments.

The AIM is intended to fulfill two purposes - operation as a general purpose reconfigurable processor by operating on data supplied by an external instrument or sensor, and also as an engineering experiment. On Fedsat the AIM will operate as an engineering experiment. The AIM will operate in a standalone manner and not be dependent on an external system to supply data to it. The AIM will demonstrate the techniques required for managing FPGA configuration files, and collect data on how often the Xilinx configuration memory upsets. For operation as a general purpose reconfigurable processor, an input interface has been included to allow data to be directly inputted to the Xilinx for processing, and an output interface has been included to allow the processed results to be fed back to the instrument.

In addition, the AIM must include interfaces to the Fedsat spacecraft bus, including command and data handling system interfaces and power system.

## IV. AIM Architecture

A block diagram of the AIM is shown in figure 1. Flash memory stores configurations and software that is unique to each configuration. EEPROM memory stores boot code. SRAM is used to hold executing code and data. The Xilinx FPGA operates under the control of the microprocessor, which loads configurations into it from flash memory. A readback circuit makes use of the readback feature that can be placed into the Xilinx. This feature can serially read out Xilinx configuration data as well as the state of application flip-flops in the FPGA. The Xilinx chip specification is fairly restrictive about how the readback is performed; it must take place at a rate between 1 and 2 Mbits per second. A rate of 1.5 Mbits per second is used in the AIM. A key feature of the Xilinx is that the readback takes place with no effect on the normal operation of the chip.

The reconfigurable processor section of the AIM (XQR4062 FPGA) operates as a slave processor to the AIM microprocessor. The microprocessor selected (UTMC 80C196) is a moderate performance 16-bit processor. The selection of radiation-hardened microprocessors is extremely limited. A 16-bit processor was selected because a 32-bit processor (typified by the Synova Mongoose-V and Lockheed Martin R6000), with its associated memories, would dissipate too much power and be too costly (>$30,000), while an 8-bit processor (typified by the Intersil 80C85 and UTMC 80C51) would not offer sufficient performance to store the readback data while responding to the spacecraft command and data handling interfaces. The 80C196 offers sufficient throughput (1-2 MIPs) to perform the operations associated with configuration and readback, with enough processing throughput leftover to handle second level processing, data formatting, and other software tasks. Low cost software development tools are available for it. For many reconfigurable processor applications it would be desirable to use a DSP chip instead of a 16-bit processor, but the cost, power, and volume constraints on the AIM precluded the use of a DSP chip.

The 80C196 processor natively addresses only 64K bytes each of code and data. Since one Xilinx configuration file alone contains 179,227 bytes, the effective memory space of the processor was increased with the use of a memory controller in an Actel FPGA. A paging scheme was implemented which allows different banks of physical memory to be mapped into the upper 32k bytes of both code and data spaces. Separate code and data page registers are implemented in the memory controller for this purpose. The lower 32K bytes of each space remain unpaged. A total of 8 code pages can be addressed, and 282 data pages.

The AIM includes interfaces to allow instrument or sensor data to be pumped directly into the Xilinx for processing. The Xilinx can use the data to generate control signals going back to the instrument (for example, to steer a mirror). The Xilinx is connected to the processor data bus as a memory mapped peripheral, so processed data can also be read by the microprocessor for further processing, formatting, and possibly for transfer to the spacecraft. In standalone mode operation (used on Fedsat), data can either be received from the spacecraft through the command interface, or simulated in software. The processor will write the data the Xilinx for processing, and read the results back out.

A 32Kx8 SRAM is connected to the Xilinx to store intermediate results and coefficients that might be required for some algorithms. The initial AIM design used the processor SRAM for this purpose, which would have required the Xilinx to take over the processor data bus as needed. The use of a separate SRAM eliminated bus grant logic and removed the possibility of a Xilinx upset from hanging the processor.

An important part of the use of the AIM on Fedsat is the collection of SEU data on Xilinx configuration memory and user/application memory. This is done by reading back the configuration memory (and optionally the user memory) in the Xilinx, and comparing it to the original configuration kept in flash memory. The readback is performed using a combination of circuitry in an Actel and software. To start the readback process, the processor generates a pulse to put the Xilinx in readback mode and start the readback circuit in the Actel FPGA. The Actel implements dual 128-bit shift registers. Xilinx readback serial data is loaded into one of the shift registers at a time. When the shift register is full, an interrupt is generated to the microprocessor and readback data is then fed into the other shift register. During this time the microprocessor can read out the data as eight 16-bit words and store them in SRAM. When the second shift register is filled, another interrupt is generated and data is again loaded into the first shift register. A complete readout of the configuration bits (a total of 1,433,812 bits) takes about 1 second. When the readout is complete, the software compares the complete readout stored in SRAM to the original configuration stored in flash memory. The software takes into account some minor formatting differences between the configuration data loaded into the Xilinx and the readback data.

## V. Physical Characteristics

The preliminary AIM flight board layout is shown in figure 2. The electronics are packaged as a single board mounted in a chassis. The chassis is 16 cm x 17.5 cm x 3.0 cm and weighs approximately 1 kilogram. Measured power on the breadboard is 2.5W from +28V. The flight model AIM will be tested for operation down to –30°C and up to +60°C. It is designed to operate after a radiation total dose exposure of at least 15K rads.

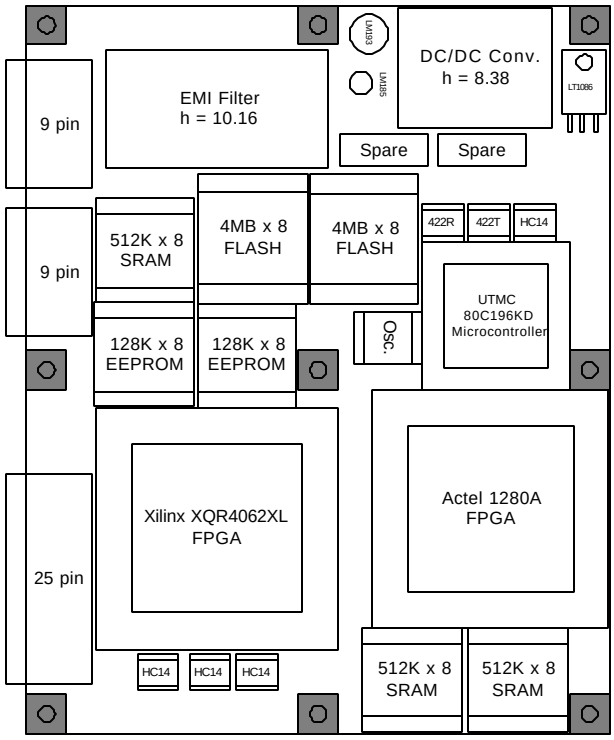


Figure 2 AIM Preliminary Flight Board Layout

## VI. Radiation Effects

The processor selected is radiation tolerant, and fairly resistant to SEUs. The EEPROM is highly SEU resistant, especially since it will only be read from in flight. The flash memory might upset, but this can be detected with the use of checksums on blocks of memory, and can be reloaded if necessary. The 32Kx8 SRAM is immume to upsets. The 512Kx8 SRAM is expected to have 3 errors per device-day for continuous operation during solar max conditions. Given that 256 Kbytes of SRAM is dedicated to code, and 1 hour of operation per day, this translates into one SEU-induced code error every 128 days of operation. Errors should actually be less frequent, because less than half the code space will probably be used. Circuitry in the Actel FPGA is implemented exclusively with the relatively SEU-resistant C-modules, not the SEU susceptible S-modules. Parts were selected to meet the Fedsat total dose requirement of 15K rads. Shielding will be used on the Actel and 512Kx8 SRAM to boost their radiation total dose tolerance to at least 15K rads. All other parts are at hard to at least 15K rads. No parts in the AIM are susceptible to single event latchup, which can result in device destruction. A list of the semiconductor parts in the AIM is shown in Table 1.

| |
|---|
| UTMC 80C196 Microprocessor |
| Xilinx XQR4062XL |
| Actel A1280A Fuse Programmed FPGA |
| SEI 29F0408RP Flash Memory |
| SEI 28C010TRPFB-15 EEPROM Memory |
| Q-Tech 48 MHz Oscillator |
| Interpoint SFMC-461 EMI Filter |
| Interpoint SMHF2805S DC/DC Converter |
| Linear Technology LT1086 Voltage Regulator |
| Fairchild 54AC14 |
| Fairchild 54AC74 |
| Intersil HS26C32 |
| Intersil HS26C31 |
| National LM193H/833 |
| National LM185BH/883 |
| Analog Devices AD590 Temperature Transducer |
| Lockheed Martin 32Kx8 SRAM |
| Motorola/Austin 5C512K8F 512Kx8 SRAM |

Table 1 AIM Part List

## VII. Next Generation Reconfigurable Processor

While rad-hard SRAM configured FPGAs are under development, they will always lag behind commercially derived FPGAs in gate count. So, the techniques developed for the AIM will be needed to take advantage of the latest FPGAs for space. The next version of the AIM might attempt to be more application oriented, less oriented towards the collection of engineering data, and de-coupled from a particular processor. The collection of upset statistics would not be important, but correcting any SEU induced configuration memory errors is needed to maintain proper device operation. A design that would meet these goals is shown in figure 3.

In this design, the AIM is a module that can be placed on a board. The module includes flash memory for storage of one or more configurations. The Actel FPGA contains a controller that automatically reads out the configuration data and compares it to the original in the flash memory. If an error is detected, the Actel will reload the Xilinx with the correct configuration. The Actel would also have a memory mapped interface to the system processor that would allow the processor to load in new configurations and report status information to the processor. A system could

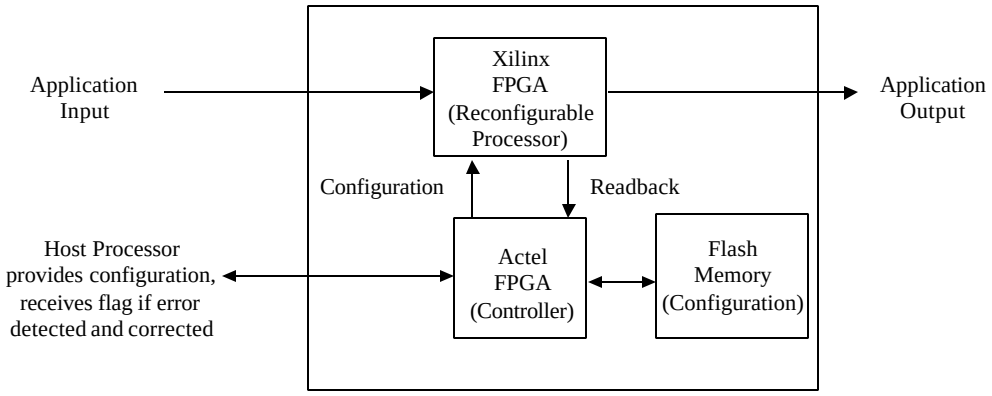


Figure 3 Next Generation AIM Module

contain one or modules depending on the amount of processing required.

## VIII. CONCLUSION

Ultimately, the primary motivation for using an AIM is cost reduction compared to implementing a comparable design with standard (non-reconfigurable) logic. The cost of repairing design errors is minimized because a corrected design can be loaded anytime, even after launch. The cost of building flight hardware can be reduced because the same AIM hardware design can be used for different applications by loading in the desired configuration. Previous attempts at designing a generic processor board for space flight applications were typically not widely used. The AIM should achieve better results because both the hardware and software can be customized.

## ACKNOWLEDGEMENTS

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