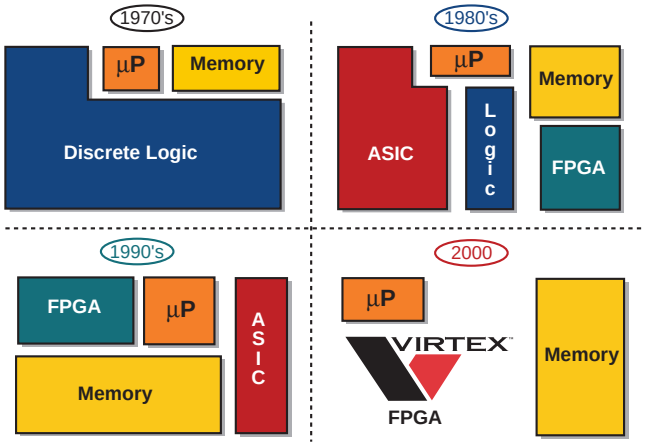
Q-Pro - for the Aerospace & Defense market

With densities up to one million system gates, Virtex QPRO™ devices provide an off-the-shelf system-level ASIC solution, without the non-recurring engineering costs, long prototype cycles, and minimum volumes required of custom ASICs.

by Howard Bogrow, Marketing Manager, Aerospace and Defense Products, Xilinx, Inc., howard@xilinx.com

The Aerospace and Defense market has been undergoing significant changes in recent years, and continues to challenge both system designers and component suppliers. Designers no longer have to specify mil-spec parts for every application, and as a result numerous mil-spec suppliers have exited the market. Thus, it has become increasingly difficult for aerospace and defense customers to obtain many needed devices. Additionally the use of custom or semi-custom ASICs may no longer be a viable option.

Even with all the changes that are taking place, the aerospace and defense market still has some unique product and supply chain requirements:



Design Evolution Using FPGAs

- **Operating temperature range** - This is typically a harsh operating environment, and while many new designs are able to use industrial temperature components, there are still numerous applications that require guaranteed performance over a wider temperature range. QPRO Virtex FPGAs provide this guarantee.
- **Packaging** - Many new applications are able to take advantage of the more cost-effective plastic packages. The QPRO Virtex family offers a wide range of solutions for these applications in both flat pack and ball grid technology. However, ceramic packaging is still available for those applications that require hermeticity, such as shipboard and space. The latest addition to our hermetic package offering is the CG560, a ceramic surface mount column grid array, which is available for the XQV1000 device.
- **COTS and DMS** - There is a very strong trend towards the use of COTS (commercial off-the-shelf) components, and away from custom or specially processed parts. Also, a big concern is DMS (diminished material supply) or product obsolescence. The QPRO Virtex family are COTS products in every sense of the definition. They are commercially available standard products that require no special processing or specifications. And,

because the QPRO Virtex family is now available with up to 1,000,000 system gates, the functions of many obsolete components such as discrete logic, semi-custom ASICs, processors, memories, and interface chips can now be incorporated into a single QPRO Virtex FPGA.

- **IP Cores** - Many aerospace and defense systems use a PowerPC architecture, and military versions of the peripherals for this processor have become very difficult to obtain. To address this problem Eureka Technologies of Los Altos, California, has developed an IP core solution that can be incorporated into QPRO Virtex devices. This core includes a PowerPC bus master and slave, PCI host bridge, bus arbiter, SDRAM controller, DMA controller, and UART.

Device	System Gates	Packages
XQV100	100,000	PQ240, BG256, CB228
XQV300	300,000	PQ240, BG352, BG432, CB228
XQV600	600,000	HQ240, BG432, CB228
XQV1000	1,000,000	BG560, CG560

Table 1 - QPRO Virtex Product Offering

Summary

QPRO Virtex devices provide unsurpassed flexibility as a replacement for ASICs for the aerospace and defense market. These products offer system-level integration and performance, and because they are reconfigurable, field upgrades are possible. QPRO Virtex FPGAs bring state-of-the-art technology to this market, while solving the critical supply management issues.

SEU Mitigation Techniques for Virtex FPGAs in Space Applications

SRAM-based logic devices such as FPGAs have some susceptibility to Single Event Upsets (SEU) and functional interruption. This paper describes several reliable mitigation techniques for the Virtex series FPGA architecture, which will retain functional integrity while static upsets are detected and corrected.

Additionally, this paper demonstrates how an SEU in an FPGA can be corrected in 3us without disrupting operation of the device, how to build hardened voting circuits, and that a single event has only 1 chance out of 3.25 million of causing a functional interrupt.

Re-configurable computing and adaptive hardware is an emerging technology for space applications. The basis for this technology is the capability for device- and system-level functional changes to be implemented in-system and transmitted remotely. FPGAs provide an array of logic resources, which may be interconnected, and configured for specific functions. All logic definitions and block connections are controlled by static RAM cells. Thus, this technology is sometimes referred to as "SRAM Logic," which allows for on-the-fly reconfiguration of the circuits' functional definition.

The Xilinx XQVR product line is a radiation-tolerant version of the of the commercially popular Virtex series FPGA. Virtex has become a common ASIC replacement in commercial markets due to its density, performance, and wide range of capabilities. The XQVR utilizes an epitaxial process that renders it latch-up immune to an LET of 125MeV-cm2/mg.

This is an excerpt of a paper presented by Carl Carmichael, Xilinx Applications Engineer, at the 1999 MAPLD Conference, held at Johns Hopkins University. For the complete paper, go to http://www.xilinx.com/products/hirel_qml.htm