XC9500XL Versus MAX7000A Architecture Comparison

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Overview

This discussion focuses on comparing the Xilinx XC9500XL CPLD family with the Altera MAX7000A (including MAX7000AE) family. Both families address the high speed 3.3V ISP CPLD marketplace, where new developments in low voltage systems demand new solutions from CPLDs. The newer XC9500XL architecture may be viewed as a functional superset of the older Max7000A base architecture, and it provides more architectural flexibility, more logic resources, and higher level of quality and reliability for new leading edge 3.3V systems.

Introduction

The Xilinx XC9500XL and Altera MAX7000A are leading complex programmable logic devices (CPLDs) developed for new 3.3 V digital systems. Compared to the older MAX7000A base architecture, the newer XC9500XL architecture incorporates many architecture features to provide more logic resources, and increased device flexibility. This provides an added level of security for designs that may be subjected to unexpected design changes throughout the product life-cycle.

The XC9500XL family is also fabricated in a newer, leading-edge FLASH process technology (in contrast to the older EEPROM technology used in the MAX7000A), which provides a higher level of device quality and reliability. Compared to the MAX7000A family the XC9500XL devices achieves 2x higher data retention and 100X higher reprogramming reliability.

High Level Architectural Comparison

MAX7000A and XC9500XL architectures have similar high level functions, so it is relatively easy to compare them based on important differences. For instance, both block the macrocells into groups - Function Blocks (FBs) on the XC9500XL family and Logic Array Blocks (LABs) on the MAX family. MAX parts group together 16 macrocells in each LAB and XC9500XL parts group 18 macrocells together. Similarly, both family part numbers include the macrocell count, so relative density comparison is easy. The equivalent XC9500XL are always 12.5% larger in macrocell capability. For example, the XC95144XL can be compared to the EPM7128A, with 144 and 128 macrocells respectively.

Both families interconnect among their respective macrocell blocks with a global interconnect structure. XC9500XL FastCONNECT II switch matrix is a high speed matrix providing more than 2 times the signal connect opportunity than the MAX 7000A family PIA for equivalent devices. The abundance of XC9500XL connections is a direct result of the smaller FastFLASH cell technology. Xilinx development system software automatically makes connections and interprets user supplied constraints to assign performance as needed.

Function Block Compare

The XC9500XL Function Block has 54 inputs and 18 macrocell outputs and may be viewed as a “54V18” block. In contrast, the MAX7000A uses “36V16” blocks (called Logic Array Block, or LAB). The XC9500XL block provides two more macrocells per Function Block for more logic “headroom”, and allows many types of look-a-head digital operations of 16-bit functions to be implemented more efficiently.

The substantially wider block fan-in also allows functions up to 54 inputs to be implemented in one logic pass for the fastest pin-to-pin performance. This is important for fast address decode functions common in today’s digital systems. The wide fan-in also effectively eliminates pin-locking issues due to block fan-in limitations. In contrast, the block fan-in limitation of the MAX7000A allows only 36-input functions to be implemented.

Macrocell Compare

The XC9500XL macrocell may be viewed as a superset of the Max7000A macrocell. Both have a set of five native product terms, p-term sets, resets and clocks. Both support edge triggered clocks. But, important differences exist in how these resources are provided. Let's focus on a few key differences: product term export/import, clocking flexibility and flip-flop configuration.

Product Term Allocation

It is vital for CPLD architecture to accept changes while maintaining pin assignments. A key adjustment is the number of product terms at the flip-flops, for state machines. Both architectures do this by finding unused p-terms at one site and reconnect them where needed. This product-term allocation process is called “expanding” by Altera. Expanding is offered two ways - parallel and shareable. Shareable expanders are unused p-terms that route back through the

LAB for reassignment. This approach comes with a relatively large penalty - three nanoseconds on the fastest speed grade parts. The parallel approach is to collect unused neighbor macrocell product terms.

Altera's parallel expanders introduce a restrictive bias. The 16 macrocells of an LAB are organized into two subgroups of eight. The first macrocell in a subgroup forwards unused p-terms to its adjacent neighbor with a small time delay adder. If not needed here, unused second macrocell p-terms get added and the batch forwards to the third macrocell (with another time delay adder). This process proceeds, if needed down to the last macrocell in the subgroup. The second subgroup of eight starts over. There is a first macrocell forwarding to the second, etc. It is important to note that only a one p-term function is possible if its p-terms are allocated to its adjacent neighbor.

This introduces a subtle bias (imbalance) into the macrocell capabilities. The first macrocell cannot obtain parallel expansion. The eighth macrocell gets up to 28 imported product terms. The eighth macrocell is potentially abundant and the first is typically depleted. The pattern repeats for the second subgroup. The problem of imbalance is that a function located at macrocell #1 must obtain more p-terms some other way, which may be shareable expanders or soft buffers (i.e., other buried macrocells) elsewhere. Both approaches add substantial timing penalty.

In contrast, XC9500XL parts offer a more powerful capability. The macrocells are not blocked into subgroups. Each macrocell has an adjacent neighbor - above and below. Every macrocell has the same neighbor relationship. First and last macrocells, are circular neighbors. Product terms can be individually passed in either direction. End macrocell bias is eliminated. A secondary benefit to the XC9500XL approach is that identical macrocell capabilities deliver superior synthesis solutions.

Clocking Flexibility

Today's processor and bus interfaces typically require a minimum of two global clocks. The MAX 7000A architecture provides 2 global clocks with inversion at the global level. Additional clocking flexibility requires the p-term clock.

XC9500XL parts have three global clocks (as well as optional product term clocks) and can select polarity at each macrocell. Hence, from one clock pin, both clock phases are available to each macrocell. The other global clocks are also available to each macrocell (either phase). Both phases of the product term clock are also available to each macrocell.

Flip Flop Configuration

D flip flops are standard in CPLDs today. CPLDs are frequently used for control operations requiring strong state machine capability. The most common state machine is the synchronous counter. Counters are best built with T flip-flops, reducing the transition logic to an AND gate. MAX 7000A only has a D flip-flop. The MAX 7000A flip flop inefficiently uses its logic to form counters. This is not the case with the XC9500XL. Here, a programmable bit alters the D configuration to a T flip-flop - without wasting macrocell logic. XC9500XL counters are then built with minimum logic and leaving more p-terms for other functions.

Interconnect Compare

The XC9500XL FastCONNECT II switch matrix provides substantially more routing switches than the MAX 7000A PIA switch. The extra routing resource ensure more robust pin-locking capability for the XC9500XL, while maintaining a uniform high-speed connection structure.

JTAG Compare

The XC9500XL devices provide a more complete set of IEEE 1149.1 STD boundary-scan instructions. (See Table 1).

The JTAG TAP Pins (TMS, TCK, TDI, and TDO) are dedicated to boundary-scan and in-system programming operations. This allows all user pins to be accessed via boundary-scan and allows the device to be reprogrammed from any configuration.

In contrast the MAX7000A has shared user I/O and JTAG TAP pins, which are user-configured. The shared pins make the MAX7000A devices susceptible to unrecoverable misprogramming (due to noise or pattern errors), whereby the device has inappropriate I/O definitions with the ISP/JTAG pins disabled (a condition known as "ISP Lock-Out").

JTAG Instruction	XC9500XL	MAX 7000A
Sample/Preload	X	X
Extest	X	X
Bypass	X	X
Intest	X	
Clamp	X	
High-Z	X	
IDCODE	X	X
USERCODE	X	X
ISP instructions	X	X

Table 1: Standard JTAG Instruction Comparison

I/O Pin Compare

The XC9500XL user I/O pins provide input hysteresis and bus-hold capabilities for improved system integrity. In comparison, the MAX7000A devices provide pull-up resistors that are activated only during in-system programming operations.

Practical Issues

Power Supply Sequencing

Mixed voltage systems bring along the challenge of sequencing the power supplies. Many CMOS technologies cannot tolerate having voltages applied to their pins without prior application of VCC to the chip. The classic result is a destructive condition called “latchup.” Xilinx XC9500XL parts were designed to tolerate power supply sequencing in any order, without damaging the Xilinx parts. In contrast, the Max7000A literature continues to recommend that the device power be applied before pins may be driven as of this writing.

Monotonic Power Supply

XC9500XL parts are designed for arbitrary sequencing and give proper behavior once the power supply is up and stable.

Many CPLDs, including the Max7000A devices, guarantee correct configuration with well-defined initial register status only if the V_{CC} power-up is monotonic. Unfortunately, this ideal power-up condition may be difficult to achieve in many cases.

Quality and Reliability Considerations

Like Flash memory devices, modern CPLDs may be programmed and reprogrammed many times within the system. Valid system operation is guaranteed only when the device can be reliably programmed each time, and the device can maintain the programming pattern (internal pattern of charged and uncharged nodes) with minimal charge leakage throughout the life of the system. Each programming operation imposes a small amount of stress at the corresponding memory cell location, whose effects accumulate to increase charge leakage and possibly cause cell failure. The reliability characteristics associated with programming and charge leakage are specified by endurance and data retention ratings, respectively, for both Flash memory devices and CPLDs.

The reliability of CPLDs is an increasingly larger part of overall system integrity for several reasons. First, CPLDs are being programmed within the system instead of being externally programmed and tested prior to board assembly. While an in-system programming failure is relatively uncommon in properly designed systems, any programming failure involves not only the device cost but also expensive board rework costs as well. Second, leading-edge manufacturers are continuing to increase the operating life of new digital systems. This puts a strain on older CPLD technologies developed for a system life of ten years or less. Finally, more systems are incorporating field upgrade capability as part of increased system life. In these systems, the programming environment is in the field under variable conditions, and the utmost programming reliability becomes critical for successful field reprogramming.

Endurance

The industry-standard measure of programming reliability is endurance, which is the minimum number of program/erase cycles the device is guaranteed to operate within datasheet specifications. The endurance rating serves two key purposes - as a quantitative limit of recommended reprogramming cycles for proper device operation, and as a qualitative measure of underlying reliability of the device. A leading Flash memory vendor notes that the failure rate on any given programming cycle is inversely proportional to the endurance rating. In this case, it is possible to consider the parameter equal to one divided by the endurance as the “average degradation per program cycle.”

Each XC9500XL device is specified for the highest endurance available for CPLDs (currently at 10,000 program/erase cycles). In contrast, the Max7000A devices are currently specified for 100 program/erase cycles (the industry minimum for in-system programmable CPLDs), or a average degradation rating for 1% per programming cycle. In comparison, the XC9500XL devices offer *two orders of magnitude* higher programming reliability than the Max7000A device during any given programming operation.

Contrary to popular misconception, there is no additional device manufacturing costs associated with providing a high level of endurance *if the underlying process technology can support that level of reliability without significant yield fallout*. The scrapping of substandard devices is the only significant manufacturing cost of providing higher quality and reliability.

Data Retention

In non-volatile memories and CPLDs, device programming is accomplished by forcing electrons to traverse an electrical insulator to charge up a floating node. The state of each programmable cell is determined by whether its floating node is electrically neutral or has a population of trapped electrons. While it is impossible for all the trapped electrons to remain within the floating node indefinitely, the leakage rate is so low that properly developed CPLDs retain their programming data in excess of 10 or more years under recommended operating conditions. This length of time is specified as the data retention.

Each XC9500XL device is guaranteed for the data retention of 20 years, while the Max7000A devices are only specified for the industry-minimum of 10 years. A longer data retention is an indication of more robust and reliable underlying technology, and allows the device to operate more reliably in a given environment than a device with a lower data retention level.

As with other quality and reliability measures, there are no additional device manufacturing costs associated with providing a high level of data retention *if the underlying process technology can support that level of reliability without significant yield fallout.*

While both CPLD families provide 3.3V in-system programming operation, the newer and more advanced XC9500XL family offers higher architectural flexibility, more logic resources, and a superior level of quality and reliability than the Max7000A families.

Conclusion

The Xilinx XC9500XL CPLD architecture is compared to the Altera Max 7000A and Max7000AE architectures.

Feature	XC9500XL	Max 7000A (including Max 7000AE)
Global Functionality		
# Global Clocks	3	2
# Global Set/Reset	Yes	Reset Only
Macrocell Block	**Function Block**	**Logic Array Block**
# Macrocells	18	16
# Block Inputs	54	36
Macrocell		
Base # P-Terms	5	5
Max P-Terms/Macrocell	90	32
Flip-flop Configuration	D/T	D only
Clock Enable	Yes	Yes
Local Clock Polarity	Yes	No
P-Term Allocation	2-D, groups of 18	1-D, groups of 8
JTAG Support		
# Instructions	8	5
Dedicated JTAG Pins	Yes	No
Electrical		
Endurance	10,000 cycles	100 cycles
Charge Retention	20 years	10 years
Voltage Compatibility	5/3.3/2.5 V	5/3.3/2.5 V
Technology	FLASH	EEPROM

Table 2: Comparison Summary