# Using the Virtex SelectI/O

XAPP133 (v2.1) January 19, 1999 Application Note


## Summary

The Virtex FPGA series includes a highly configurable, high-performance I/O resource, called SelectI/O™ to provide support for a wide variety of I/O standards. The SelectI/O resource is a robust set of features including programmable control of output drive strength, slew rate, and input delay and hold time. Taking advantage of the flexibility and SelectI/O features and the design considerations described in this document can improve and simplify system level design. Appendix A is the Virtex-E SelectI/O Update. Appendix B is the Virtex-E LVDS SelectI/O design guide.


## Introduction

As FPGAs continue to grow in size and capacity, the larger and more complex systems designed for them demand an increased variety of I/O standards. Furthermore, as system clock speeds continue to increase, the need for high performance I/O becomes more important. While chip-to-chip delays have an increasingly substantial impact on overall system speed, the task of achieving the desired system performance becomes more difficult with the proliferation of low-voltage I/O standards. SelectI/O, the revolutionary input/output resources of Virtex devices, has resolved this potential problem by providing a highly configurable, high-performance alternative to the I/O resources of more conventional programmable devices. The Virtex SelectI/O features combine the flexibility and time-to-market advantages of programmable logic with the high performance previously available only with ASICs and custom ICs.

Each SelectI/O block can support up to 16 I/O standards. Supporting such a variety of I/O standards allows the support of a wide variety of applications, from general purpose standard applications to high-speed low-voltage memory busses.

SelectI/O blocks also provide selectable output drive strengths and programmable slew rates for the LVTTL output buffers, as well as an optional, programmable weak pull-up, weak pull-down, or weak "keeper" circuit ideal for use in external bussing applications.

Each Input/Output Block (IOB) includes three registers, one each for the input, output, and 3-state signals within the IOB. These registers are optionally configurable as either a D-type flip-flop or as a level sensitive latch.

The input buffer has an optional delay element used to guarantee a zero hold time requirement for input signals registered within the IOB.

The Virtex SelectI/O features also provide dedicated resources for input reference voltage ($V_{REF}$) and output source voltage ($V_{CCO}$), along with a convenient banking system that simplifies board design.

By taking advantage of the built-in features and wide variety of I/O standards supported by the SelectI/O features, system-level design and board design can be greatly simplified and improved.

## Fundamentals

Modern bus applications, pioneered by the largest and most influential companies in the digital electronics industry, are commonly introduced with a new I/O standard tailored specifically to the needs of that application. The bus I/O standards provide specifications to other vendors

who create products designed to interface with these applications. Each standard often has its own specifications for current, voltage, I/O buffering, and termination techniques.

The ability to provide the flexibility and time-to-market advantages of programmable logic is increasingly dependent on the capability of the programmable logic device to support an ever increasing variety of I/O standards

The SelectI/O resources feature highly configurable input and output buffers which provide support for a wide variety of I/O standards. An input buffer can be configured as either a simple buffer or as a differential amplifier input. An output buffer can be configured as either a Push-Pull output or as an Open Drain output. As shown in Table 1, each buffer type can support a variety of current and voltage requirements.

**Table 1: SelectI/O Supported Standards (Typical Values)**

| I/O Standard | Input Reference Voltage ($V_{REF}$) | Output Source Voltage ($V_{CCO}$) | Board Termination Voltage ($V_{TT}$) |
|---|---|---|---|
| LVTTL | N/A | 3.3 | N/A |
| LVCMOS2 | N/A | 2.5 | N/A |
| PCI | N/A | 3.3 | N/A |
| GTL | 0.8 | N/A | 1.2 |
| GTL+ | 1.0 | N/A | 1.5 |
| HSTL Class I | 0.75 | 1.5 | 0.75 |
| HSTL Class III | 0.9 | 1.5 | 0.75 |
| HSTL Class IV | 0.9 | 1.5 | 0.75 |
| SSTL3 Class I and II | 1.5 | 3.3 | 1.5 |
| SSTL2 Class I and II | 1.25 | 2.5 | 1.25 |
| CTT | 1.5 | 3.3 | 1.5 |
| AGP-2X | 1.32 | 3.3 | N/A |

## Overview of Supported I/O Standards

This section provides a brief overview of the I/O standards supported by all Virtex devices.

While most I/O standards specify a range of allowed voltages, this document records typical voltage values only. Detailed information on each specification may be found on the Electronic Industry Alliance Jedec website at: **http://www.jedec.org**

### LVTTL — Low-Voltage TTL

The Low-Voltage TTL, or LVTTL standard is a general purpose EIA/JESDSA standard for 3.3V applications that uses an LVTTL input buffer and a Push-Pull output buffer. The input and output buffers are both 5V-tolerant. This standard requires a 3.3V output source voltage ($V_{CCO}$), but does not require the use of a reference voltage ($V_{REF}$) or a termination voltage ($V_{TT}$).

### LVCMOS2 — Low-Voltage CMOS for 2.5 Volts

The Low-Voltage CMOS for 2.5 Volts or lower, or LVCMOS2 standard is an extension of the LVCMOS standard (JESD 8.-5) used for general purpose 2.5V applications. It uses a 5V-tolerant CMOS input buffer and a Push-Pull output buffer. This standard requires a 2.5V output source voltage ($V_{CCO}$), but does not require the use of a reference voltage ($V_{REF}$) or a board termination voltage ($V_{TT}$).

### PCI — Peripheral Component Interface

The Peripheral Component Interface, or PCI standard specifies support for both 33 MHz and 66 MHz PCI bus applications. It uses a LVTTL input buffer and a Push-Pull output buffer. This standard does not require the use of a reference voltage ($V_{REF}$) or a board termination voltage ($V_{TT}$), however, it does require a 3.3V output source voltage ($V_{CCO}$). SelectI/O devices configured as PCI, 33 Mhz, 5V SelectI/O are also 5V tolerant.

### GTL — Gunning Transceiver Logic Terminated

The Gunning Transceiver Logic, or GTL standard is a high-speed bus standard (JESD8.3) invented by Xerox. Xilinx has implemented the terminated variation for this standard. This standard requires a differential amplifier input buffer and a Open Drain output buffer.

### GTL+ — Gunning Transceiver Logic Plus

The Gunning Transceiver Logic Plus, or GTL+ standard is a high-speed bus standard (JESD8.3) first used by the Pentium Pro processor.

### HSTL — High-Speed Transceiver Logic

The High-Speed Transceiver Logic, or HSTL standard is a general purpose high-speed, 1.5V bus standard sponsored by IBM (EIA/JESD 8-6). This standard has four variations or classes. SelectI/O devices support Class I, III, and IV. This standard requires a Differential Amplifier input buffer and a Push-Pull output buffer.

### SSTL3 — Stub Series Terminated Logic for 3.3V

The Stub Series Terminated Logic for 3.3V, or SSTL3 standard is a general purpose 3.3V memory bus standard also sponsored by Hitachi and IBM (JESD8-8). This standard has two classes, I and II. SelectI/O devices support both classes for the SSTL3 standard. This standard requires a Differential Amplifier input buffer and an Push-Pull output buffer.

### SSTL2 — Stub Series Terminated Logic for 2.5V

The Stub Series Terminated Logic for 2.5V, or SSTL2 standard is a general purpose 2.5V memory bus standard sponsored by Hitachi and IBM (JESD8-9). This standard has two classes, I and II. SelectI/O devices support both classes for the SSTL2 standard. This standard requires a Differential Amplifier input buffer and an Push-Pull output buffer.

### CTT — Center Tap Terminated

The Center Tap Terminated, or CTT standard is a 3.3V memory bus standard sponsored by Fujitsu (JESD8-4). This standard requires a Differential Amplifier input buffer and a Push-Pull output buffer.

### AGP-2X — Advanced Graphics Port

The Intel AGP standard is a 3.3V Advanced Graphics Port-2X bus standard used with the Pentium II processor for graphics applications. This standard requires a Push-Pull output buffer and a Differential Amplifier input buffer.

## Library Symbols

The Xilinx library includes an extensive list of symbols designed to provide support for the variety of SelectI/O features. Most of these symbols represent variations of the five generic SelectI/O symbols.

- IBUF (input buffer)
- IBUFG (global clock input buffer)
- OBUF (output buffer)
- OBUFT (3-state output buffer)
- IOBUF (input/output buffer)

### IBUF

Signals used as inputs to the Virtex device must source an input buffer (IBUF) via an external input port. The generic Virtex IBUF symbol appears in Figure 1. The extension to the base name defines which I/O standard the IBUF uses. The assumed standard is LVTTL when the generic IBUF has no specified extension.

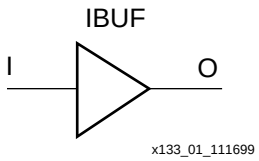


**Figure 1: Input Buffer (IBUF) Symbol**

The following list details the variations of the IBUF symbol:

- IBUF
- IBUF_LVCMOS2
- IBUF_PCI33_3
- IBUF_PCI33_5
- IBUF_PCI66_3
- IBUF_GTL
- IBUF_GTLP
- IBUF_HSTL_I
- IBUF_HSTL_III
- IBUF_HSTL_IV
- IBUF_SSTL3_I
- IBUF_SSTL3_II
- IBUF_SSTL2_I
- IBUF_SSTL2_II
- IBUF_CTT
- IBUF_AGP

When the IBUF symbol supports an I/O standard that does not require a differential amplifier input (LVTTL, LVCMOS2, or PCI33_5), the IBUF automatically configures as a 5V-tolerant input buffer unless the $V_{CCO}$ for the bank is less than 2V. If the single-ended IBUF is placed in a bank with an HSTL standard ($V_{CCO}$ < 2V), the input buffer is not 5V-tolerant.

When the IBUF symbol supports an I/O standard that requires a differential amplifier input, the IBUF automatically configures as a differential amplifier input buffer. The low-voltage I/O standards with a differential amplifier input require an external reference voltage input $V_{REF}$. In this case the input buffer is not 5V-tolerant.

The voltage reference signal is “banked” within the Virtex device on a half-edge basis such that for all packages there are eight independent $V_{REF}$ banks internally. See Figure 2 for a representation of the Virtex I/O banks. Within each bank approximately one of every six I/O pins is automatically configured as a $V_{REF}$ input. After placing a differential amplifier input signal within a given $V_{REF}$ bank, the same external source must drive all I/O pins configured as a $V_{REF}$ input.

IBUF placement restrictions require that any differential amplifier input signals within a bank be of the same standard. How to specify a specific location for the IBUF via the LOC property is described below. Table 2 summarizes the Virtex input standards compatibility requirements.

An optional delay element is associated with each IBUF. When the IBUF drives a flip-flop within the IOB, the delay element by default activates to ensure a zero hold-time requirement. The NODELAY=TRUE property overrides this default.

When the IBUF does not drive a flip-flop within the IOB, the delay element de-activates by default to provide higher performance. To delay the input signal, activate the delay element with the DELAY=TRUE property.

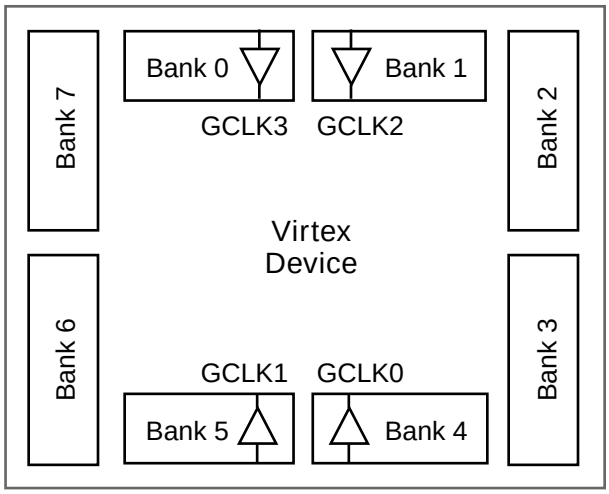


**Figure 2: Virtex I/O Banks**

**Table 2: Xilinx Input Standards Compatibility Requirements**

| | |
|---|---|
| Rule 1 | All differential amplifier input signals within a bank are required to be of the same standard. |
| Rule 2 | There are no placement restrictions for inputs with standards that require a single-ended input buffer. |

## IBUFG

Signals used as high fanout clock inputs to the Virtex device should drive a global clock input buffer (IBUFG) via an external input port in order to take advantage of one of the four dedicated global clock distribution networks. The output of the IBUFG symbol can only drive a CLKDLL, CLKDLLHF, or a BUFG symbol. The generic Virtex IBUFG symbol appears in Figure 3.

### Symbol

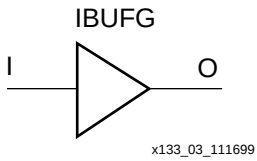


**Figure 3: Virtex Global Clock Input Buffer (IBUFG)**

The extension to the base name determines which I/O standard is used by the IBUFG. With no extension specified for the generic IBUFG symbol, the assumed standard is LVTTL.

The following list details variations of the IBUFG symbol.

- IBUFG
- IBUFG_LVCMOS2
- IBUFG_PCI33_3
- IBUFG_PCI33_5
- IBUFG_PCI66_3
- IBUFG_GTL
- IBUFG_GTLP
- IBUFG_HSTL_I
- IBUFG_HSTL_III
- IBUFG_HSTL_IV

- IBUFG_SSTL3_I
- IBUFG_SSTL3_II
- IBUFG_SSTL2_I
- IBUFG_SSTL2_II
- IBUFG_CTT
- IBUFG_AGP

When the IBUFG symbol supports an I/O standard that requires a differential amplifier input, the IBUFG automatically configures as a differential amplifier input buffer. The low-voltage I/O standards with a differential amplifier input require an external reference voltage input $V_{REF}$.

The voltage reference signal is “banked” within the Virtex device on a half-edge basis such that for all packages there are eight independent $V_{REF}$ banks internally. See Figure 2 for a representation of the Virtex I/O banks. Within each bank approximately one of every six I/O pins is automatically configured as a $V_{REF}$ input. After placing a differential amplifier input signal within a given $V_{REF}$ bank, the same external source must drive all I/O pins configured as a $V_{REF}$ input.

IBUFG placement restrictions require any differential amplifier input signals within a bank be of the same standard. The LOC property can specify a location for the IBUFG.

As an added convenience, the BUFGP can be used to instantiate a high fanout clock input. The BUFGP symbol represents a combination of the LVTTL IBUFG and BUFG symbols, such that the output of the BUFGP can connect directly to the clock pins throughout the design.

Unlike previous architectures, the Virtex BUFGP symbol can only be placed in a global clock pad location. The LOC property can specify a location for the BUFGP.

## OBUF

An OBUF must drive outputs through an external output port. The generic output buffer (OBUF) symbol appears in Figure 4.

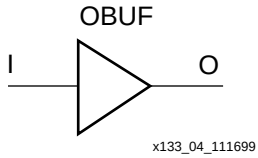


**Figure 4: Virtex Output Buffer (OBUF) Symbol**

The extension to the base name defines which I/O standard the OBUF uses. With no extension specified for the generic OBUF symbol, the assumed standard is slew rate limited LVTTL with 12 mA drive strength.

The LVTTL OBUF additionally can support one of two slew rate modes to minimize bus transients. By default, the slew rate for each output buffer is reduced to minimize power bus transients when switching non-critical signals.

LVTTL output buffers have selectable drive strengths.

The format for LVTTL OBUF symbol names is as follows.

OBUF_<slew_rate>_<drive_strength>

<slew_rate> is either F (Fast), or S (Slow) and <drive_strength> is specified in mA (2, 4, 6, 8, 12, 16, or 24).

The following list details variations of the OBUF symbol.

- OBUF
- OBUF_S_2
- OBUF_S_4
- OBUF_S_6

- OBUF_S_8
- OBUF_S_12
- OBUF_S_16
- OBUF_S_24
- OBUF_F_2
- OBUF_F_4
- OBUF_F_6
- OBUF_F_8
- OBUF_F_12
- OBUF_F_16
- OBUF_F_24
- OBUF_LVCMOS2
- OBUF_PCI33_3
- OBUF_PCI33_5
- OBUF_PCI66_3
- OBUF_GTL
- OBUF_GTLP
- OBUF_HSTL_I
- OBUF_HSTL_III
- OBUF_HSTL_IV
- OBUF_SSTL3_I
- OBUF_SSTL3_II
- OBUF_SSTL2_I
- OBUF_SSTL2_II
- OBUF_CTT
- OBUF_AGP

All Virtex packages, except for the PQ, HQ and CS packages provide at least sixteen fixed $V_{CCO}$ pins, two for each $V_{CCO}$ bank within the device. The Virtex PQ and HQ packages support only one $V_{CCO}$ bank. The Virtex-E series supports eight banks for the HQ and PQ packages. The CS packages support four $V_{CCO}$ banks.

OBUF placement restrictions require that within a given $V_{CCO}$ bank each OBUF share the same output source drive voltage. Input buffers of any type and output buffers that do not require $V_{CCO}$ can be placed within any $V_{CCO}$ bank. Table 3 summarizes the Virtex output compatibility requirements. The LOC property can specify a location for the OBUF.

**Table 3: Output Standards Compatibility Requirements**

| | |
|---|---|
| Rule 1 | Only outputs with standards which share compatible $V_{CCO}$ may be used within the same bank. |
| Rule 2 | There are no placement restrictions for outputs with standards that do not require a $V_{CCO}$. |
| $V_{CCO}$ | Compatible Standards |
| 3.3 | PCI, LVTTL, SSTL3_I, SSTL3_II, CTT, AGP, GTL, GTL+ |
| 2.5 | SSTL2_I, SSTL2_II, LVCMOS2, GTL, GTL+ |
| 1.5 | HSTL_I, HSTL_III, HSTL_IV, GTL, GTL+ |

## OBUFT

The generic 3-state output buffer OBUFT, shown in Figure 5, typically implements 3-state outputs or bidirectional I/O.

The extension to the base name defines which I/O standard OBUFT uses. With no extension specified for the generic OBUFT symbol, the assumed standard is slew rate limited LVTTL with 12 mA drive strength.

The LVTTL OBUFT additionally can support one of two slew rate modes to minimize bus transients. By default, the slew rate for each output buffer is reduced to minimize power bus transients when switching non-critical signals.

LVTTL 3-state output buffers have selectable drive strengths.

The format for LVTTL OBUFT symbol names is as follows.

OBUFT_<slew_rate>_<drive_strength>

<slew_rate> can be either F (Fast), or S (Slow) and <drive_strength> is specified in mA (2, 4, 6, 8, 12, 16, or 24).

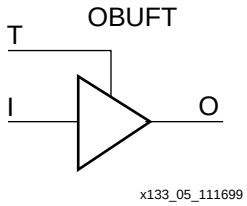


**Figure 5: 3-State Output Buffer Symbol (OBUFT)**

The following list details variations of the OBUFT symbol.

- OBUFT
- OBUFT_S_2
- OBUFT_S_4
- OBUFT_S_6
- OBUFT_S_8
- OBUFT_S_12
- OBUFT_S_16
- OBUFT_S_24
- OBUFT_F_2
- OBUFT_F_4
- OBUFT_F_6
- OBUFT_F_8
- OBUFT_F_12
- OBUFT_F_16
- OBUFT_F_24
- OBUFT_LVCMOS2
- OBUFT_PCI33_3
- OBUFT_PCI33_5
- OBUFT_PCI66_3
- OBUFT_GTL
- OBUFT_GTLP
- OBUFT_HSTL_I

- OBUFT_HSTL_III
- OBUFT_HSTL_IV
- OBUFT_SSTL3_I
- OBUFT_SSTL3_II
- OBUFT_SSTL2_I
- OBUFT_SSTL2_II
- OBUFT_CTT
- OBUFT_AGP

All Virtex packages except for the PQ and HQ packages provide at least sixteen fixed $V_{CCO}$ pins, two for each $V_{CCO}$ bank within the device. The Virtex PQ and HQ packages support only one $V_{CCO}$ bank. The Virtex-E series supports eight banks for the HQ and PQ packages. The CS package supports four $V_{CCO}$ banks.

The SelectI/O OBUFT placement restrictions require that within a given $V_{CCO}$ bank each OBUFT share the same output source drive voltage. Input buffers of any type and output buffers that do not require $V_{CCO}$ can be placed within the same $V_{CCO}$ bank.

The LOC property can specify a location for the OBUFT.

3-state output buffers and bidirectional buffers can have either a weak pull-up resistor, a weak pull-down resistor, or a weak “keeper” circuit. Control this feature by adding the appropriate symbol to the output net of the OBUFT (PULLUP, PULLDOWN, or KEEPER).

The weak “keeper” circuit requires the input buffer within the IOB to sample the I/O signal. So, OBUFTs programmed for an I/O standard that requires a $V_{REF}$ have automatic placement of a $V_{REF}$ in the bank with an OBUFT configured with a weak “keeper” circuit. This restriction does not affect most circuit design as applications using an OBUFT configured with a weak “keeper” typically implement a bidirectional I/O. In this case the IBUF (and the corresponding $V_{REF}$) are explicitly placed.

The LOC property can specify a location for the OBUFT.

## IOBUF

Use the IOBUF symbol for bidirectional signals that require both an input buffer and a 3-state output buffer with an active high 3-state pin. The generic input/output buffer IOBUF appears in Figure 6.

The extension to the base name defines which I/O standard the IOBUF uses. With no extension specified for the generic IOBUF symbol, the assumed standard is LVTTL input buffer and slew rate limited LVTTL with 12 mA drive strength for the output buffer.

The LVTTL IOBUF additionally can support one of two slew rate modes to minimize bus transients. By default, the slew rate for each output buffer is reduced to minimize power bus transients when switching non-critical signals.

LVTTL bidirectional buffers have selectable output drive strengths.

The format for LVTTL IOBUF symbol names is as follows.

IOBUF_<slew_rate>_<drive_strength>

<slew_rate> can be either F (Fast), or S (Slow) and <drive_strength> is specified in mA (2, 4, 6, 8, 12, 16, or 24).

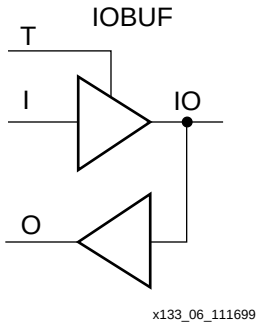


**Figure 6: Input/Output Buffer Symbol (IOBUF)**

The following list details variations of the IOBUF symbol.

- IOBUF
- IOBUF_S_2
- IOBUF_S_4
- IOBUF_S_6
- IOBUF_S_8
- IOBUF_S_12
- IOBUF_S_16
- IOBUF_S_24
- IOBUF_F_2
- IOBUF_F_4
- IOBUF_F_6
- IOBUF_F_8
- IOBUF_F_12
- IOBUF_F_16
- IOBUF_F_24
- IOBUF_LVCMOS2
- IOBUF_PCI33_3
- IOBUF_PCI33_5
- IOBUF_PCI66_3
- IOBUF_GTL
- IOBUF_GTLP
- IOBUF_HSTL_I
- IOBUF_HSTL_III
- IOBUF_HSTL_IV
- IOBUF_SSTL3_I
- IOBUF_SSTL3_II
- IOBUF_SSTL2_I
- IOBUF_SSTL2_II
- IOBUF_CTT
- IOBUF_AGP

When the IOBUF symbol used supports an I/O standard that does not require a differential amplifier input (LVTTL, LVCMOS2, or PCI33_5), and the $V_{CCO}$ within the given I/O bank is greater than 2V, the IOBUF automatically configures with a 5V-tolerant input buffer. If placing the single-ended IOBUF in a bank with an HSTL standard ($V_{CCO}$ < 2V), the IOBUF input buffer is not 5V-tolerant.

When the IOBUF symbol used supports an I/O standard that requires a differential amplifier input, the IOBUF automatically configures with a differential amplifier input buffer. The low-voltage I/O standards with a differential amplifier input require an external reference voltage input $V_{REF}$.

The voltage reference signal is “banked” within the Virtex device on a half-edge basis such that for all packages there are eight independent $V_{REF}$ banks internally. See Figure 2 on page 5 for a representation of the Virtex I/O banks. Within each bank approximately one of every six I/O pins is automatically configured as a $V_{REF}$ input. After placing a differential amplifier input signal within a given $V_{REF}$ bank, the same external source must drive all I/O pins configured as a $V_{REF}$ input.

IOBUF placement restrictions require any differential amplifier input signals within a bank be of the same standard.

All Virtex packages except for the PQ and HQ packages provide at least 16 fixed $V_{CCO}$ pins, two for each $V_{CCO}$ bank within the device. The Virtex PQ and HQ packages support only one $V_{CCO}$ bank. The Virtex-E series supports eight banks for the HQ and PQ packages. The CS package supports four $V_{CCO}$ banks.

Additional restrictions on the Virtex SelectI/O IOBUF placement require that within a given $V_{CCO}$ bank each IOBUF must share the same output source drive voltage. Input buffers of any type and output buffers that do not require $V_{CCO}$ can be placed within the same $V_{CCO}$ bank. The LOC property can specify a location for the IOBUF.

An optional delay element is associated with the input path in each IOBUF. When the IOBUF drives an input flip-flop within the IOB, the delay element activates by default to ensure a zero hold-time requirement. Override this default with the NODELAY=TRUE property.

In the case when the IOBUF does not drive an input flip-flop within the IOB, the delay element de-activates by default to provide higher performance. To delay the input signal, activate the delay element with the DELAY=TRUE property.

3-state output buffers and bidirectional buffers can have either a weak pull-up resistor, a weak pull-down resistor, or a weak “keeper” circuit. Control this feature by adding the appropriate symbol to the output net of the IOBUF (PULLUP, PULLDOWN, or KEEPER).

## SelectI/O Properties

Access to some of the SelectI/O features (for example, location constraints, input delay, output drive strength, and slew rate) is available through properties associated with these features.

### Input Delay Properties

An optional delay element is associated with each IBUF. When the IBUF drives a flip-flop within the IOB, the delay element activates by default to ensure a zero hold-time requirement. Use the NODELAY=TRUE property to override this default.

In the case when the IBUF does not drive a flip-flop within the IOB, the delay element by default de-activates to provide higher performance. To delay the input signal, activate the delay element with the DELAY=TRUE property.

### IOB Flip-Flop/Latch Property

The Virtex series IO Block (IOB) includes an optional register on the input path, an optional register on the output path, and an optional register on the 3-state control pin. The design implementation software automatically takes advantage of these registers when the following option for the Map program is specified.

```
map -pr b <filename>
```

Alternatively, the IOB = TRUE property can be placed on a register to force the mapper to place the register in an IOB.

### Location Constraints

Specify the location of each SelectI/O symbol with the location constraint LOC attached to the SelectI/O symbol. The external port identifier indicates the value of the location constrain. The format of the port identifier depends on the package chosen for the specific design.

The LOC properties use the following form.

LOC=A42

LOC=P37

### Output Slew Rate Property

As mentioned above, a variety of symbol names provide the option of choosing the desired slew rate for the output buffers. In the case of the LVTTL output buffers (OBUF, OBUFT, and IOBUF), slew rate control can be alternatively programed with the SLEW= property. By default, the slew rate for each output buffer is reduced to minimize power bus transients when switching non-critical signals. The SLEW= property has one of the two following values.

SLEW=SLOW (Default)

SLEW=FAST

#### Output Drive Strength Property

The desired output drive strength can be additionally specified by choosing the appropriate library symbol. The Xilinx library also provides an alternative method for specifying this feature. For the LVTTL output buffers (OBUF, OBUFT, and IOBUF, the desired drive strength can be specified with the DRIVE= property. This property could have one of the following seven values.

DRIVE=2

DRIVE=4

DRIVE=6

DRIVE=8

DRIVE=12 (Default)

DRIVE=16

DRIVE=24

## Design Considerations

While the SelectI/O features are easy to use, attention to the following design considerations can help avoid pitfalls and improve success.

### Reference Voltage ($V_{REF}$) Pins

Low-voltage I/O standards with a differential amplifier input buffer require an input reference voltage ($V_{REF}$). Provide the $V_{REF}$ as an external signal to the device.

The voltage reference signal is “banked” within the device on a half-edge basis such that for all packages there are eight independent $V_{REF}$ banks internally. See Figure 2 on page 5 for a representation of the Virtex I/O banks. Within each bank approximately one of every six I/O pins is automatically configured as a $V_{REF}$ input. After placing a differential amplifier input signal within a given $V_{REF}$ bank, the same external source must drive all I/O pins configured as a $V_{REF}$ input.

Within each $V_{REF}$ bank, any input buffers that require a $V_{REF}$ signal must be of the same type. Output buffers of any type and input buffers can be placed without requiring a reference voltage within the same $V_{REF}$ bank.

## Output Drive Source Voltage ($V_{CCO}$) Pins

Many of the low voltage I/O standards supported by SelectI/O devices require a different output drive source voltage ($V_{CCO}$). As a result each device can often have to support multiple output drive source voltages.

To accomplish this, all Virtex packages except for the PQ and HQ packages provide at least sixteen fixed $V_{CCO}$ pins, two for each $V_{CCO}$ bank within the device. The Virtex PQ and HQ packages support only one $V_{CCO}$ bank. The Virtex-E series supports eight banks for the HQ and PQ packages. The CS package supports four $V_{CCO}$ banks.

Output buffers within a given $V_{CCO}$ bank must share the same output drive source voltage. Input buffers of any type and output buffers can be placed without that requiring $V_{CCO}$ within any $V_{CCO}$ bank.

## Transmission Line Effects

The delay of an electrical signal along a wire is dominated by the rise and fall times when the signal travels a short distance. Transmission line delays vary with inductance and capacitance, but a well-designed board can experience delays of approximately 180 ps per inch.

Transmission line effects, or reflections, typically start at 1.5" for fast (1.5 ns) rise and fall times. Poor (or non-existent) termination or changes in the transmission line impedance cause these reflections and can cause additional delay in longer traces. As system speeds continue to increase, the effect of I/O delays can become a limiting factor and therefore transmission line termination becomes increasingly more important.

## Termination Techniques

A variety of termination techniques reduce the impact of transmission line effects.

The following lists output termination techniques.

- None
- Series
- Parallel (Shunt)
- Series and Parallel (Series-Shunt)

Input termination techniques include the following.

- None
- Parallel (Shunt)

These termination techniques can be applied in any combination. A generic example of each combination of termination methods appears in Figure 7.

## Simultaneous Switching Guidelines

Ground bounce can occur with high-speed digital ICs when multiple outputs change states simultaneously, causing undesired transient behavior on an output, or in the internal logic. This problem is also referred to as the Simultaneous Switching Output (SSO) problem.

Ground bounce is primarily due to current changes in the combined inductance of ground pins, bond wires, and ground metallization. The IC internal ground level deviates from the external system ground level for a short duration (a few nanoseconds) after multiple outputs change state simultaneously.

Ground bounce affects stable Low outputs and all inputs because they interpret the incoming signal by comparing it to the internal ground. If the ground bounce amplitude exceeds the actual instantaneous noise margin, then a non-changing input can be interpreted as a short pulse with a polarity opposite to the ground bounce.

Table 4 provides the guidelines for the maximum number of simultaneously switching outputs allowed per output power/ground pair to avoid the effects of ground bounce. Refer to Table 5 for the number of effective output power/ground pairs for each Virtex device and package combination.

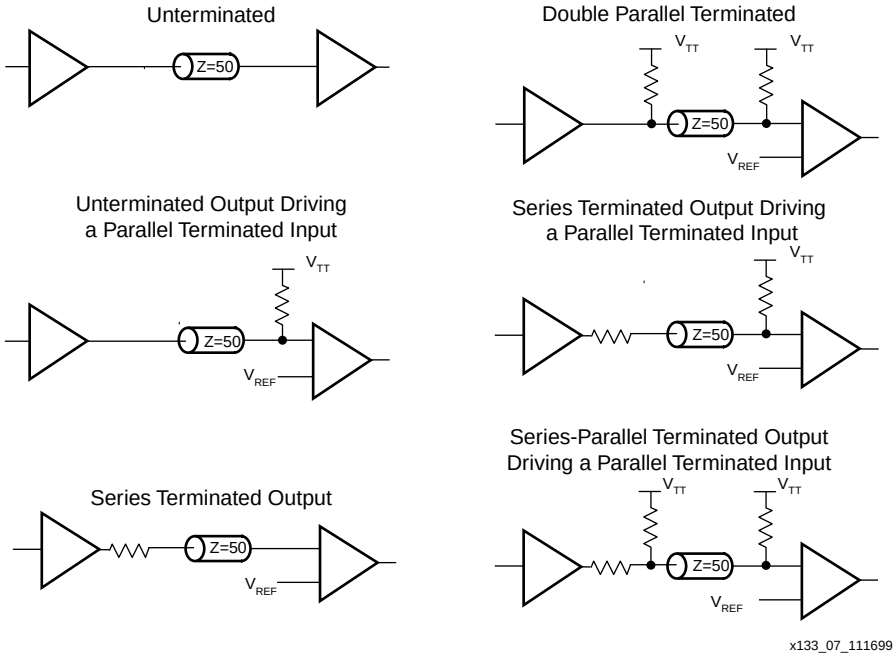


**Figure 7: Overview of Standard Input and Output Termination Methods**

**Table 4: Guidelines for Maximum Number of Simultaneously Switching Outputs per Power/Ground Pair**

| | Package | | |
|---|---|---|---|
| **Standard** | **BGA, CS, FGA** | **HQ** | **PQ, TQ** |
| LVTTL Slow Slew Rate, 2 mA drive | 68 | 49 | 36 |
| LVTTL Slow Slew Rate, 4 mA drive | 41 | 31 | 20 |
| LVTTL Slow Slew Rate, 6 mA drive | 29 | 22 | 15 |
| LVTTL Slow Slew Rate, 8 mA drive | 22 | 17 | 12 |
| LVTTL Slow Slew Rate, 12 mA drive | 17 | 12 | 9 |
| LVTTL Slow Slew Rate, 16 mA drive | 14 | 10 | 7 |
| LVTTL Slow Slew Rate, 24 mA drive | 9 | 7 | 5 |
| LVTTL Fast Slew Rate, 2 mA drive | 40 | 29 | 21 |
| LVTTL Fast Slew Rate, 4 mA drive | 24 | 18 | 12 |
| LVTTL Fast Slew Rate, 6 mA drive | 17 | 13 | 9 |
| LVTTL Fast Slew Rate, 8 mA drive | 13 | 10 | 7 |
| LVTTL Fast Slew Rate, 12 mA drive | 10 | 7 | 5 |
| LVTTL Fast Slew Rate, 16 mA drive | 8 | 6 | 4 |
| LVTTL Fast Slew Rate, 24 mA drive | 5 | 4 | 3 |
| LVCMOS2 | 10 | 7 | 5 |
| PCI | 8 | 6 | 4 |
| GTL | 4 | 4 | 4 |
| GTL+ | 4 | 4 | 4 |
| HSTL Class I | 18 | 13 | 9 |
| HSTL Class III | 9 | 7 | 5 |
| HSTL Class IV | 5 | 4 | 3 |
| SSTL2 Class I | 15 | 11 | 8 |
| SSTL2 Class II | 10 | 7 | 5 |
| SSTL3 Class I | 11 | 8 | 6 |
| SSTL3 Class II | 7 | 5 | 4 |
| CTT | 14 | 10 | 7 |
| AGP | 9 | 7 | 5 |

**Note:**
1. This analysis assumes a 35 pF load for each output.

**Table 5: Effective Output Power/Ground Pairs for Virtex Devices**

| | Virtex Devices | | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|
| **Package** | **V50** | **V100** | **V150** | **V200** | **V300** | **V400** | **V600** | **V800** | **V1000** |
| CS144 | 12 | 12 | | | | | | | |
| TQ144 | 8 | 8 | | | | | | | |
| PQ240 | 16 | 16 | 16 | 16 | 16 | | | | |
| HQ240 | | | | | | 16 | 16 | 16 | |
| BG256/FG256 | 15 | 20 | 24 | 24 | | | | | |
| BG352 | | | 26 | 32 | 32 | | | | |
| BG432 | | | | | 32 | 40 | 40 | 48 | |
| FG456 | | | 28 | 40 | 40 | | | | |
| BG560 | | | | | | 48 | 48 | 56 | 56 |
| FG676 | | | | | | 54 | 56 | 58 | |
| FG680 | | | | | | | 46 | 52 | 60 |

### 5-V Tolerant I/O

The following lists the Virtex SelectI/O standards for which the input and output buffers are 5V tolerant:

- LVTTL
- LVCMOS2
- PCI33_5

The 3V PCI I/O standards do not include 5V tolerant input and output buffers.

## Application Examples

Creating a design with the SelectI/O features requires the instantiation of the desired library symbol within the design code. At the board level, designers need to know the termination techniques required for each I/O standard.

This section describes some common application examples illustrating the termination techniques recommended by each of the standards supported by the SelectI/O features.

### Termination Examples

Circuit examples involving typical termination techniques for each of the SelectI/O standards follow. For a full range of accepted values for the DC voltage specifications for each standard, refer to the table associated with each figure.

The resistors used in each termination technique example and the transmission lines depicted represent board level components and are not meant to represent components on the device.

### GTL

A sample circuit illustrating a valid termination technique for GTL is shown in Figure 8. Table 6 lists DC voltage specifications.

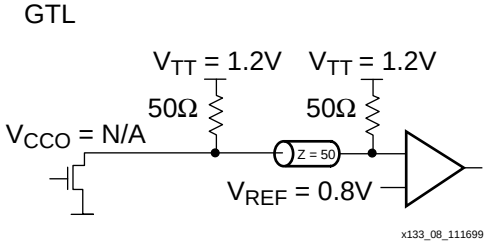


**Figure 8: GTL Terminated**

**Table 6: GTL Voltage Specifications**

| Parameter | Min | Typ | Max |
|---|---|---|---|
| $V_{CCO}$ | - | N/A | - |
| $V_{REF} = N \times V_{TT}$[1] | 0.74 | 0.8 | 0.86 |
| $V_{TT}$ | 1.14 | 1.2 | 1.26 |
| $V_{IH} = V_{REF} + 0.05$ | 0.79 | 0.85 | - |
| $V_{IL} = V_{REF} – 0.05$ | - | 0.75 | 0.81 |
| $V_{OH}$ | - | - | - |
| $V_{OL}$ | - | 0.2 | 0.4 |
| $I_{OH}$ at $V_{OH}$(mA) | - | - | - |
| $I_{OL}$at $V_{OL}$(mA) at 0.4V | 32 | - | - |
| $I_{OL}$at $V_{OL}$(mA) at 0.2V | - | - | 40 |

**Note:**
1. N must be greater than or equal to 0.653 and less than or equal to 0.68.

## GTL+

A sample circuit illustrating a valid termination technique for GTL+ appears in Figure 9. DC voltage specifications appear in Table 7.

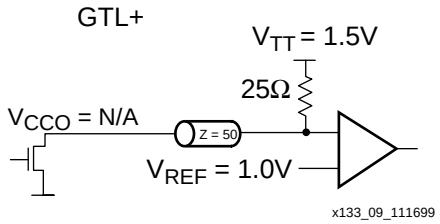


**Figure 9: GTL+**

**Table 7: GTL+ Voltage Specifications**

| Parameter | Min | Typ | Max |
|---|---|---|---|
| $V_{CCO}$ | - | - | - |
| $V_{REF} = N \times V_{TT}$[1] | 0.88 | 1.0 | 1.12 |
| $V_{TT}$ | 1.35 | 1.5 | 1.65 |
| $V_{IH} = V_{REF} + 0.2$ | 1.08 | 1.2 | - |
| $V_{IL} = V_{REF} - 0.2$ | - | 0.8 | 0.92 |
| $V_{OH}$ | - | - | - |
| $V_{OL}$ | 0.3 | 0.45 | 0.6 |
| $I_{OH}$ at $V_{OH}$ (mA) | - | - | - |
| $I_{OL}$at $V_{OL}$ (mA) at 0.6V | 36 | - | - |
| $I_{OL}$at $V_{OL}$ (mA) at 0.3V | - | - | 48 |

**Note:**

1. N must be greater than or equal to 0.653 and less than or equal to 0.68.

## HSTL

A sample circuit illustrating a valid termination technique for HSTL_I appears in Figure 10.A sample circuit illustrating a valid termination technique for HSTL_III appears in Figure 11.

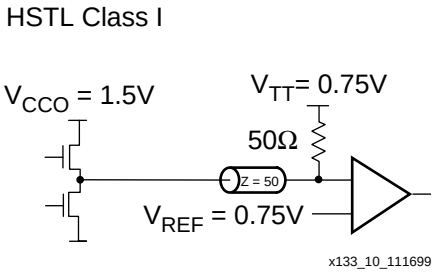


**Figure 10: Terminated HSTL Class I**

**Table 8: HSTL Class I Voltage Specification**

| Parameter | Min | Typ | Max |
|---|---|---|---|
| $V_{CCO}$ | 1.40 | 1.50 | 1.60 |
| $V_{REF}$ | 0.68 | 0.75 | 0.90 |
| $V_{TT}$ | | $V_{CCO} \times 0.5$ | |
| $V_{IH}$ | $V_{REF}$ + 0.1 | | |
| $V_{IL}$ | | | $V_{REF}$ – 0.1 |
| $V_{OH}$ | $V_{CCO}$ – 0.4 | | |
| $V_{OL}$ | | | 0.4 |
| $I_{OH}$ at $V_{OH}$ (mA) | –8 | - | - |
| $I_{OL}$at $V_{OL}$ (mA) | 8 | - | - |

HSTL Class III

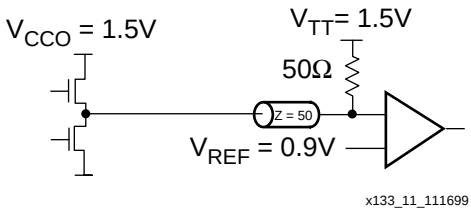


**Figure 11: Terminated HSTL Class III**

**Table 9: HSTL Class III Voltage Specification**

| Parameter | Min | Typ | Max |
|---|---|---|---|
| $V_{CCO}$ | 1.40 | 1.50 | 1.60 |
| $V_{REF}$ (1) | | 0.90 | |
| $V_{TT}$ | | $V_{CCO}$ | |
| $V_{IH}$ | $V_{REF}$ + 0.1 | | |
| $V_{IL}$ | | | $V_{REF}$ – 0.1 |
| $V_{OH}$ | $V_{CCO}$ – 0.4 | | |
| $V_{OL}$ | | | 0.4 |
| $I_{OH}$ at $V_{OH}$ (mA) | –8 | - | - |
| $I_{OL}$at $V_{OL}$ (mA) | 24 | - | - |

**NOTE:**

1. Per EIA/JESD8-6, "The value of $V_{REF}$ is to be selected by the user to provide optimum noise margin in the use conditions specified by the user."

A sample circuit illustrating a valid termination technique for HSTL_IV appears in Figure 12.

HSTL Class IV

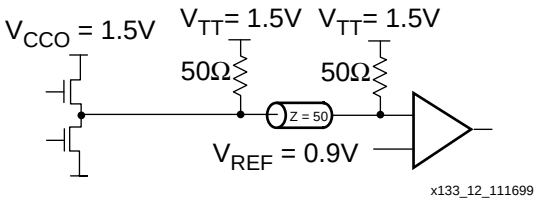


**Figure 12: Terminated HSTL Class IV**

**Table 10: HSTL Class IV Voltage Specification**

| Parameter | Min | Typ | Max |
|---|---|---|---|
| $V_{CCO}$ | 1.40 | 1.50 | 1.60 |
| $V_{REF}$ | | 0.90 | |
| $V_{TT}$ | | $V_{CCO}$ | |
| $V_{IH}$ | $V_{REF}$ + 0.1 | | |
| $V_{IL}$ | | | $V_{REF}$ – 0.1 |
| $V_{OH}$ | $V_{CCO}$ – 0.4 | | |
| $V_{OL}$ | | | 0.4 |
| $I_{OH}$ at $V_{OH}$ (mA) | –8 | - | - |
| $I_{OL}$at $V_{OL}$ (mA) | 48 | - | - |

**NOTE:**
1. Per EIA/JESD8-6, "The value of $V_{REF}$ is to be selected by the user to provide optimum noise margin in the use conditions specified by the user.

## SSTL3_I

A sample circuit illustrating a valid termination technique for SSTL3_I appears in Figure 13. DC voltage specifications appear in Table 11.

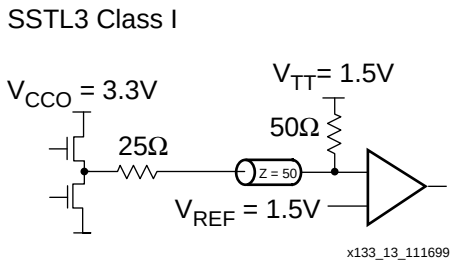


**Figure 13: Terminated SSTL3 Class I**

**Table 11: SSTL3_I Voltage Specifications**

| Parameter | Min | Typ | Max |
|---|---|---|---|
| $V_{CCO}$ | 3.0 | 3.3 | 3.6 |
| $V_{REF} = 0.45 \times V_{CCO}$ | 1.3 | 1.5 | 1.7 |
| $V_{TT} = V_{REF}$ | 1.3 | 1.5 | 1.7 |
| $V_{IH} = V_{REF} + 0.2$ | 1.5 | 1.7 | 3.9(1) |
| $V_{IL} = V_{REF} – 0.2$ | –0.3(2) | 1.3 | 1.5 |
| $V_{OH} = V_{REF} + 0.6$ | 1.9 | 2.1 | - |
| $V_{OL} = V_{REF} – 0.6$ | - | 0.9 | 1.1 |
| $I_{OH}$ at $V_{OH}$ (mA) | –8 | - | - |
| $I_{OL}$at $V_{OL}$ (mA) | 8 | - | - |

**NOTE:**
1. $V_{IH}$ maximum is $V_{CCO}$ + 0.3
2. $V_{IL}$ minimum does not conform to the formula

## SSTL3_II

A sample circuit illustrating a valid termination technique for SSTL3_II appears in Figure 14. DC voltage specifications appear in Table 12.

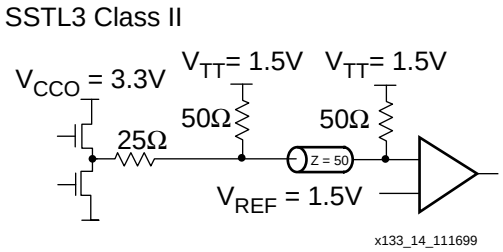


**Figure 14: Terminated SSTL3 Class II**

**Table 12: SSTL3_II Voltage Specifications**

| Parameter | Min | Typ | Max |
|---|---|---|---|
| $V_{CCO}$ | 3.0 | 3.3 | 3.6 |
| $V_{REF} = 0.45 \times V_{CCO}$ | 1.3 | 1.5 | 1.7 |
| $V_{TT} = V_{REF}$ | 1.3 | 1.5 | 1.7 |
| $V_{IH} = V_{REF} + 0.2$ | 1.5 | 1.7 | 3.9(1) |
| $V_{IL} = V_{REF} – 0.2$ | –0.3(2) | 1.3 | 1.5 |
| $V_{OH} = V_{REF} + 0.8$ | 2.1 | 2.3 | - |
| $V_{OL} = V_{REF} – 0.8$ | - | 0.7 | 0.9 |
| $I_{OH}$ at $V_{OH}$ (mA) | –16 | - | - |
| $I_{OL}$ at $V_{OL}$ (mA) | 16 | - | - |

**NOTE:**
1. $V_{IH}$ maximum is $V_{CCO}$ + 0.3
2. $V_{IL}$ minimum does not conform to the formula

## SSTL2_I

A sample circuit illustrating a valid termination technique for SSTL2_I appears in Figure 15. DC voltage specifications appear in Table 13.

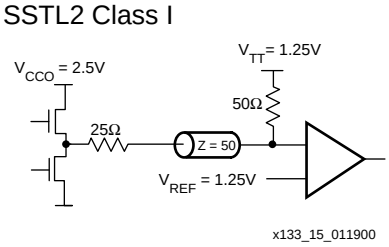


**Figure 15: Terminated SSTL2 Class I**

**Table 13: SSTL2_I Voltage Specifications**

| Parameter | Min | Typ | Max |
|---|---|---|---|
| $V_{CCO}$ | 2.3 | 2.5 | 2.7 |
| $V_{REF} = 0.5 \times V_{CCO}$ | 1.15 | 1.25 | 1.35 |
| $V_{TT} = V_{REF} + N^{(1)}$ | 1.11 | 1.25 | 1.39 |
| $V_{IH} = V_{REF} + 0.18$ | 1.33 | 1.43 | $3.0^{(2)}$ |
| $V_{IL} = V_{REF} – 0.18$ | $–0.3^{(3)}$ | 1.03 | 1.17 |
| $V_{OH} = V_{REF} + 0.05$ | 1.76 | 1.82 | 1.96 |
| $V_{OL} = V_{REF} – 0.05$ | 0.54 | 0.68 | 0.74 |
| $I_{OH}$ at $V_{OH}$ (mA) | –7.6 | - | - |
| $I_{OL}$ at $V_{OL}$ (mA) | 7.6 | - | - |

**NOTE:**
1. N must be greater than or equal to -0.04 and less than or equal to 0.04.
2. $V_{IH}$ maximum is $V_{CCO}$ + 0.3.
3. $V_{IL}$ minimum does not conform to the formula.

## SSTL2_II

A sample circuit illustrating a valid termination technique for SSTL2_II appears in Figure 16. DC voltage specifications appear in Table 14.

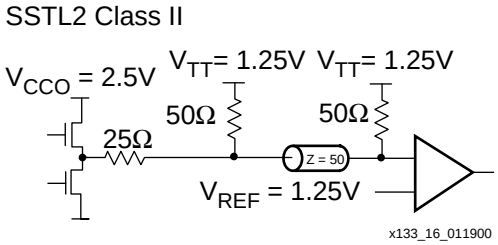


**Figure 16: Terminated SSTL2 Class II**

**Table 14: SSTL2_II Voltage Specifications**

| Parameter | Min | Typ | Max |
|---|---|---|---|
| $V_{CCO}$ | 2.3 | 2.5 | 2.7 |
| $V_{REF} = 0.5 \times V_{CCO}$ | 1.15 | 1.25 | 1.35 |
| $V_{TT} = V_{REF} + N^{(1)}$ | 1.11 | 1.25 | 1.39 |
| $V_{IH} = V_{REF} + 0.8$ | 1.33 | 1.43 | $3.0^{(2)}$ |
| $V_{IL} = V_{REF} – 0.8$ | $–0.3^{(3)}$ | 1.07 | 1.21 |
| $V_{OH}$ | 1.95 | 2.01 | - |
| $V_{OL}$ | - | 0.49 | 0.55 |
| $I_{OH}$ at $V_{OH}$ (mA) | –15.2 | - | - |
| $I_{OL}$ at $V_{OL}$ (mA) | 15.2 | - | - |

**NOTE:**
1. N must be greater than or equal to –0.04 and less than or equal to 0.04.
2. $V_{IH}$ maximum is $V_{CCO}$ + 0.3.
3. $V_{IL}$ minimum does not conform to the formula.

## CTT

A sample circuit illustrating a valid termination technique for CTT appear in Figure 17. DC voltage specifications appear in Table 15.

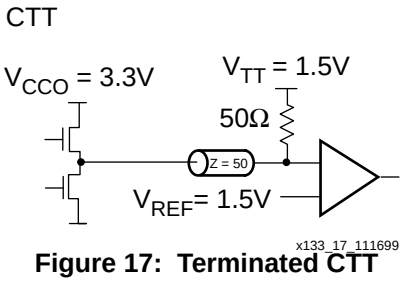


**Figure 17: Terminated CTT**

**Table 15: CTT Voltage Specifications**

| Parameter | Min | Typ | Max |
|---|---|---|---|
| $V_{CCO}$ | 2.05(1) | 3.3 | 3.6 |
| $V_{REF}$ | 1.35 | 1.5 | 1.65 |
| $V_{TT}$ | 1.35 | 1.5 | 1.65 |
| $V_{IH} = V_{REF} + 0.2$ | 1.55 | 1.7 | - |
| $V_{IL} = V_{REF} – 0.2$ | - | 1.3 | 1.45 |
| $V_{OH} = V_{REF} + 0.4$ | 1.75 | 1.9 | - |
| $V_{OL} = V_{REF} – 0.4$ | - | 1.1 | 1.25 |
| $I_{OH}$ at $V_{OH}$ (mA) | –8 | - | - |
| $I_{OL}$ at $V_{OL}$ (mA) | 8 | - | - |

**NOTE:**
1. Timing delays are calculated based on $V_{CCO}$ min of 3.0V.

## PCI33_3 & PCI66_3

PCI33_3 or PCI66_3 require no termination. DC voltage specifications appear in Table 16.

**Table 16: PCI33_3 and PCI66_3 Voltage Specifications**

| Parameter | Min | Typ | Max |
|---|---|---|---|
| $V_{CCO}$ | 3.0 | 3.3 | 3.6 |
| $V_{REF}$ | - | - | - |
| $V_{TT}$ | - | - | - |
| $V_{IH} = 0.6 \times V_{CCINT}$ | 1.425 | 1.5 | 3.6 |
| $V_{IL} = 0.4 \times V_{CCINT}$ | –0.5 | 1.0 | 1.05 |
| $V_{OH} = 0.9 \times V_{CCO}$ | 2.7 | - | - |
| $V_{OL} = 0.1 \times V_{CCO}$ | - | - | 0.36 |
| $I_{OH}$ at $V_{OH}$ (mA) | Note 1 | - | - |
| $I_{OL}$ at $V_{OL}$ (mA) | Note 1 | - | - |

**NOTE:**
1. Tested according to the relevant specification.

## PCI33_5

PCI33_5 requires no termination. DC voltage specifications appear in Table 17.

**Table 17: PCI33_5 Voltage Specifications**

| Parameter | Min | Typ | Max |
|---|---|---|---|
| $V_{CCO}$ | 3.0 | 3.3 | 3.6 |
| $V_{REF}$ | - | - | - |
| $V_{TT}$ | - | - | - |
| $V_{IH}$ | 1.425 | 1.5 | 5.5 |
| $V_{IL}$ | –0.5 | 1.0 | 1.05 |
| $V_{OH}$ | 2.4 | - | - |
| $V_{OL}$ | - | - | 0.55 |
| $I_{OH}$ at $V_{OH}$ (mA) | Note 1 | - | - |
| $I_{OL}$at $V_{OL}$ (mA) | Note 1 | - | - |

**NOTE:**
1. Tested according to the relevant specification.

## LVTTL

LVTTL requires no termination. DC voltage specifications appears in Table 18.

**Table 18: LVTTL Voltage Specifications**

| Parameter | Min | Typ | Max |
|---|---|---|---|
| $V_{CCO}$ | 3.0 | 3.3 | 3.6 |
| $V_{REF}$ | - | - | - |
| $V_{TT}$ | - | - | - |
| $V_{IH}$ | 2.0 | - | 5.5 |
| $V_{IL}$ | –0.5 | - | 0.8 |
| $V_{OH}$ | 1.9 | - | - |
| $V_{OL}$ | - | - | 0.4 |
| $I_{OH}$ at $V_{OH}$ (mA) | –24 | - | - |
| $I_{OL}$at $V_{OL}$ (mA) | 24 | - | - |

**NOTE:**
1. $V_{OL}$and $V_{OH}$ for lower drive currents are sample tested.

## LVCMOS2

LVCMOS2 requires no termination. DC voltage specifications appear in Table 19.

**Table 19: LVCMOS2 Voltage Specifications**

| Parameter | Min | Typ | Max |
|---|---|---|---|
| $V_{CCO}$ | 2.3 | 2.5 | 2.7 |
| $V_{REF}$ | - | - | - |
| $V_{TT}$ | - | - | - |
| $V_{IH}$ | 1.7 | - | 5.5 |
| $V_{IL}$ | –0.5 | - | 0.7 |
| $V_{OH}$ | 1.9 | - | - |
| $V_{OL}$ | - | - | 0.4 |
| $I_{OH}$ at $V_{OH}$ (mA) | –12 | - | - |
| $I_{OL}$at $V_{OL}$ (mA) | 12 | - | - |

## AGP-2X

The specification for the AGP-2X standard does not document a recommended termination technique. DC voltage specifications appear in Table 20.

**Table 20: AGP-2X Voltage Specifications**

| Parameter | Min | Typ | Max |
|---|---|---|---|
| $V_{CCO}$ | 3.0 | 3.3 | 3.6 |
| $V_{REF} = N \times V_{CCO}$ (1) | 1.17 | 1.32 | 1.48 |
| $V_{TT} = V_{REF}$ | 1.35 | 1.5 | 1.65 |
| $V_{IH} = V_{REF} + 0.2$ | 1.37 | 1.52 | - |
| $V_{IL} = V_{REF} – 0.2$ | - | 1.12 | 1.28 |
| $V_{OH} = 0.9 \times V_{CCO}$ | 2.7 | 3.0 | - |
| $V_{OL} = 0.1 \times V_{CCO}$ | - | 0.33 | 0.36 |
| $I_{OH}$ at $V_{OH}$ (mA) | Note 2 | - | - |
| $I_{OL}$ at $V_{OL}$ (mA) | Note 2 | - | - |

**NOTE:**
1. N must be greater than or equal to 0.39 and less than or equal to 0.41.
2. Tested according to the relevant specification.

# Appendix A: Virtex-E SelectI/O Update

The Virtex-E family of FPGAs offers four I/O standards not previously offered in the Virtex series. This appendix describes these additional I/O standards. Table 21 shows all of the I/O standards supported by the Virtex-E family.

**Table 21: I/O Standards Supported by the Virtex-E Family**

| I/O Standard | Output $V_{CCO}$ | Input $V_{CCO}$ | Input $V_{REF}$ | Board Termination Voltage ($V_{TT}$) |
|---|---|---|---|---|
| LVTTL | 3.3 | 3.3 | N/A | N/A |
| LVCMOS2 | 2.5 | 2.5 | N/A | N/A |
| LVCMOS18 | 1.8 | 1.8 | N/A | N/A |
| SSTL3 I & II | 3.3 | N/A | 1.50 | 1.50 |
| SSTL2 I & II | 2.5 | N/A | 1.25 | 1.25 |
| GTL | N/A | N/A | 0.80 | 1.20 |
| GTL+ | N/A | N/A | 1.0 | 1.50 |
| HSTL I | 1.5 | N/A | 0.75 | 0.75 |
| HSTL III & IV | 1.5 | N/A | 0.90 | 1.50 |
| CTT | 3.3 | N/A | 1.50 | 1.50 |
| AGP-2X | 3.3 | N/A | 1.32 | N/A |
| PCI33_3 | 3.3 | 3.3 | N/A | N/A |
| PCI66_3 | 3.3 | 3.3 | N/A | N/A |
| BLVDS & LVDS | 2.5 | N/A | N/A | N/A |
| LVPECL | 3.3 | N/A | N/A | N/A |

## Overview of Supported I/O Standards for Virtex-E devices

This section details the LVCMOS18, LVDS, BLVDS and LVPECL I/O standards. Other standards listed in Table 21 are described earlier in the body of this document starting on page 2.

### LVCMOS18 — 1.8 V Low Voltage CMOS

This standard is an extension of the LVCMOS standard. It is used in general purpose 1.8 V applications. The use of a reference voltage ($V_{REF}$) or a board termination voltage ($V_{TT}$) is not required.

### LVDS — Low Voltage Differential Signal

LVDS is a differential I/O standard. It requires that one data bit is carried through two signal lines. As with all differential signaling standards, LVDS has an inherent noise immunity over single-ended I/O standards. The voltage swing between two signal lines is approximately 350mV. The use of a reference voltage ($V_{REF}$) or a board termination voltage ($V_{TT}$) is not required. LVDS requires the use of two pins per input or output. LVDS requires external resistor termination.

### BLVDS — Bus LVDS

This standard allows for bidirectional LVDS communication between two or more devices. The external resistor termination is different than the one for standard LVDS.

### LVPECL — Low Voltage Positive Emitter Coupled Logic

LVPECL is another differential I/O standard. It requires two signal lines for transmitting one data bit. This standard specifies two pins per input or output. The voltage swing between these two signal lines is approximately 850 mV. The use of a reference voltage ($V_{REF}$) or a board termination voltage ($V_{TT}$) is not required. The LVPECL standard requires external resistor termination.

## Library Symbols

For a more detailed description of the Xilinx library symbols for the I/O standards please refer to the "Library Symbols" on page 3. The following SelectI/O symbols have been added to the library for support of the Virtex-E family. For guidelines on using the LVDS library symbols, please refer to "Appendix B: LVDS Design Guide" on page 30.

- IBUF_LVCMOS18
- IBUFG_LVCMOS18
- OBUF_LVCMOS18
- OBUFT_LVCMOS18
- IOBUF_LVCMOS18
- IBUF_LVDS
- IBUFG_LVDS
- OBUF_LVDS
- OBUFT_LVDS
- IOBUF_LVDS
- IBUF_LVPECL
- IBUFG_LVPECL
- OBUF_LVPECL
- OBUFT_LVPECL
- IOBUF_LVPECL

## Design Considerations

### Simultaneous Switching Guidelines

Table 22 provides the number of effective output power/ground pairs for each Virtex-E device and package combination.

**Table 22: Virtex-E Equivalent Power/Ground Pairs**

| Pkg/Part | v100e | v200e | v300e | v400e | v600e | v1000e | v1600e | v2000e |
|---|---|---|---|---|---|---|---|---|
| CS144 | 12 | 12 | | | | | | |
| PQ240 | 20 | 20 | 20 | 20 | | | | |
| HQ240 | | | | | 20 | 20 | | |
| BG432 | | | 32 | 40 | 40 | | | |
| BG560 | | | | | | 56 | 58 | 60 |
| FG256(1) | 20 | 24 | 24 | | | | | |
| FG456 | | 40 | 40 | | | | | |
| FG676 | | | | 54 | 56 | | | |
| FG680(2) | | | | | 46 | 56 | 56 | 56 |
| FG860 | | | | | | 58 | 60 | 64 |
| FG900 NYA | | | | | | | | |
| FG1156 | | | | | | 96 | 104 | 120 |

**NOTE:**
1. Virtex-E devices in FG256 packages have more $V_{CCO}$ than Virtex series devices.
2. FG680 numbers are preliminary.

## Application Examples

This section describes some common application examples illustrating the termination techniques and DC voltage specifications of the four differential I/O standards outlined in this appendix.

## LVCMOS18

LVCMOS18 does not require termination. Table 23 lists DC voltage specifications.

**Table 23: LVCMOS18 Voltage Specifications**

| Parameter | Min | Typ | Max |
|---|---|---|---|
| $V_{CCO}$ | 1.70 | 1.80 | 1.90 |
| $V_{REF}$ | - | - | - |
| $V_{TT}$ | - | - | - |
| $V_{IH}$ | 70% $V_{CCO}$ | - | 1.95 |
| $V_{IL}$ | – 0.5 | - | 20% $V_{CCO}$ |
| $V_{OH}$ | $V_{CCO}$ – 0.4 | - | - |
| $V_{OL}$ | - | - | 0.4 |
| $I_{OH}$ at $V_{OH}$ (mA) | –8 | - | - |
| $I_{OL}$at $V_{OL}$ (mA) | 8 | - | - |

## LVDS

Depending on whether the device is transmitting an LVDS signal or receiving an LVDS signal, there are two different circuits used for LVDS termination. A sample circuit illustrating a valid termination technique for transmitting LVDS signals appears in Figure 18. A sample circuit illustrating a valid termination for receiving LVDS signals appears in Figure 19. Table 24 lists DC voltage specifications. Further information on the specific termination resistor packs shown can be found on page 33.

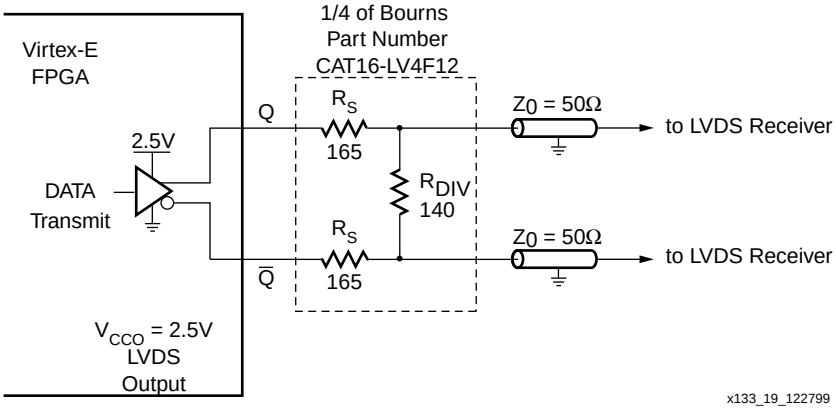


**Figure 18: Transmitting LVDS Signal Circuit**

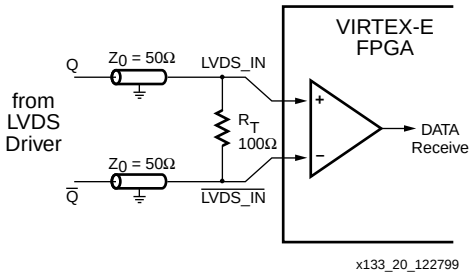


**Figure 19: Receiving LVDS Signal Circuit**

**Table 24: LVDS Voltage Specifications**

| Parameter | Min | Typ | Max |
|---|---|---|---|
| $V_{CCO}$ | 2.375 | 2.5 | 2.625 |
| $V_{ICM}$(2) | 0.2 | 1.25 | 2.2 |
| $V_{OCM}$(1) | 1.125 | 1.25 | 1.375 |
| $V_{IDIFF}$ (mV)(1) | 100 | 350 | - |
| $V_{ODIFF}$ (mV)(1) | 250 | 350 | 450 |
| $V_{OH}$(1) | 1.25 | - | - |
| $V_{OL}$(1) | - | - | 1.25 |

**NOTE:**
1. Measured with a 100 Ω resistor across Q and $\overline{Q}$.
2. Measured with a differential input voltage = ± 350 mV.

## LVPECL

Depending on whether the device is transmitting an LVPECL signal or receiving an LVPECL signal, there are two different circuits used for LVPECL termination. A sample circuit illustrating a valid termination technique for transmitting LVPECL signals appears in Figure 20. A sample circuit illustrating a valid termination for receiving LVPECL signals appears in Figure 21. Table 24 lists DC voltage specifications. Further information on the specific termination resistor packs shown can be found in the next section.

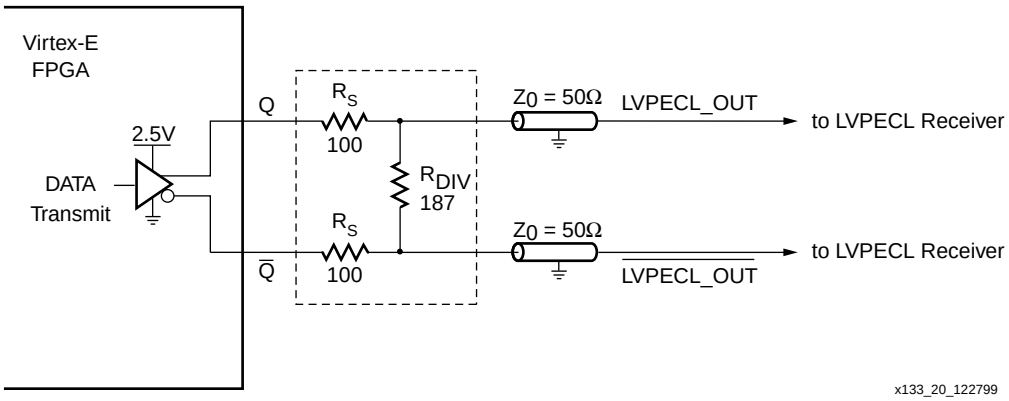


**Figure 20: Transmitting LVPECL Signal Circuit**

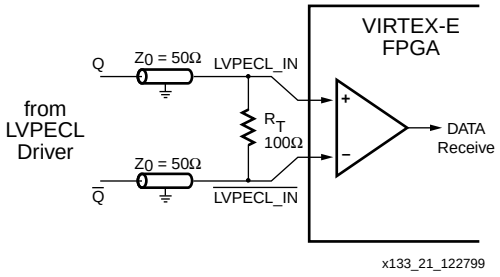


**Figure 21: Receiving LVPECL Signal Circuit**

**Table 25: LVPECL Voltage Specifications**

| Parameter | Min | Typ | Max |
|---|---|---|---|
| $V_{CCO}$ | 3.0 | 3.3 | 3.6 |
| $V_{REF}$ | - | - | - |
| $V_{TT}$ | - | - | - |
| $V_{IH}$ | 1.49 | - | 2.72 |
| $V_{IL}$ | 0.86 | - | 2.125 |
| $V_{OH}$ | 1.8 | - | - |
| $V_{OL}$ | - | - | 1.57 |

Note: For more detailed specification, please refer to the datasheet.

## Termination Resistor Packs

Resistor packs are available with the values and the configuration required for LVDS and LVPECL termination from Bourns, Inc. The part numbers listed in Table 26. For pricing and availability questions, please contact them directly at www.bourns.com.

**Table 26: LVDS and LVPECL resistor packs from Bourns Inc.**

| Bourns Part Number | Differential I/O Standard | Termination for: | Pairs per Pack | Number of Pins |
|---|---|---|---|---|
| CAT16–LV2F6 | LVDS | Driver | 2 | 8 |
| CAT16–LV4F12 | LVDS | Driver | 4 | 16 |
| CAT16–PC2F6 | LVPECL | Driver | 2 | 8 |
| CAT16–PC4F12 | LVPECL | Driver | 4 | 16 |
| CAT16–PT2F2 | LVDS/LVPECL | Receiver | 2 | 8 |
| CAT16–PT4F4 | LVDS/LVPECL | Receiver | 4 | 16 |

# Appendix B: LVDS Design Guide

The SelectI/O library elements have been expanded for Virtex-E devices to include new LVDS variants. At this time all of the cells may not be included in the Synthesis libraries. The 2.1i-Service Pack 2 update for Alliance and Foundation software includes these cells in the VHDL and Verilog libraries. It is necessary to combine these cells to create the P-side (positive) and N-side (negative) as described in the input, output, 3-state and bidirectional sections.

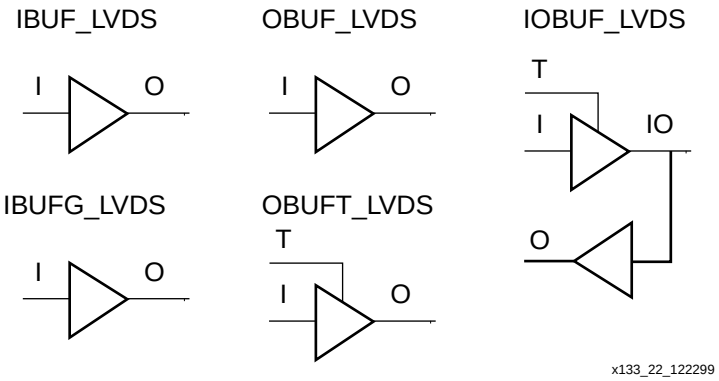


**Figure 22: LVDS elements**

## Creating an LVDS Global Clock Input Buffer

The global clock input buffer may be combined with the adjacent IOB to form an LVDS clock input buffer. The P-side resides in the GCLKPAD location and the N-side resides in the adjacent IO_LVDS_DLL site.

**Table 27: Global Clock Input Buffer Locations**

| Package | GCLKPAD3 | GCLKPAD2 | GCLKPAD1 | GCLKPAD0 |
|---|---|---|---|---|
| CS144 | C6 | B7 | M6 | N8 |
| PQ240 | P215 | P209 | P87 | P93 |
| BG432 | C17 | B16 | AL17 | AH15 |
| BG560 | C18 | E17 | AM18 | AM17 |
| FG256 | A7 | A8 | T8 | N9 |
| FG456 | B11 | D11 | AA11 | U12 |
| FG676 | B13 | F14 | AF13 | AC14 |
| FG680 | C22 | A19 | AT22 | AT21 |
| FG860 | A22 | D22 | AW21 | AW20 |
| FG900 | A15 | E16 | AH16 | AF16 |
| FG1156 | C17 | J18 | AL17 | AM18 |

### HDL Instantiation

Only one global clock input buffer is required to be instantiated in the design and placed on the correct GCLKPAD location. The N-side of the buffer will be reserved and no other IOB will be allowed to be placed on this location.

In the physical device a configuration option is enabled that routes the pad wire to the differential input buffer located in the GCLKIOB. The output of this buffer then drives the output of the GCLKIOB cell. In EPIC it will appear that the second buffer is unused. Any attempt to use this location for another purpose will cause a DRC error from the software.

**VHDL Instantiation**

```
gclk0_p : IBUFG_LVDS port map (I=>clk_external, O=>clk_internal);
```

**Verilog instantiation**

```
IBUFG_LVDS gclk0_p (.I(clk_external), .O(clk_internal));
```

### Location constraints

All LVDS buffers must be explicitly placed on a device. For the global clock input buffers this may be done with the following constraint in the .ucf or .ncf file.

```
NET clk_external LOC = GCLKPAD3;
```

GCLKPAD3 may also be replaced with the package pin name such as D17 for the BG432 package.

### Optional N-side

Some designers may prefer to also instantiate the N-side buffer for the global clock buffer. This will allow the top-level netlist to include both net connections for PCB layout and system level integration. In this case the output P-side IBUFG connection is the only one to have a net connected to it. Since the N-side IBUFG does not have a connection in the EDIF netlist it will be trimmed from the design in MAP.

**VHDL instantiation**

```
gclk0_p : IBUFG_LVDS port map (I=>clk_p_external, O=>clk_internal);
gclk0_n : IBUFG_LVDS port map (I=>clk_n_external, O=>clk_internal);
```

**Verilog instantiation**

```
IBUFG_LVDS gclk0_p (.I(clk_p_external), .O(clk_internal));
IBUFG_LVDS gclk0_n (.I(clk_n_external), .O(clk_internal));
```

### Location constraints

All LVDS buffers must be explicitly placed on a device. For the global clock input buffers this may be done with the following constraint in the .ucf or .ncf file.

```
NET clk_p_external LOC = GCLKPAD3;
NET clk_n_external LOC = C17;
```

GCLKPAD3 may also be replaced with the package pin name such as D17 for the BG432 package.

## Creating an LVDS Input Buffer

An LVDS input buffer may be placed in a wide number of IOB locations. The exact location is dependent on the package that is used. The Virtex-E package information lists the possible locations as IO_L#P for the P-side and IO_L#N for the N-side where # is the pair number.

### HDL Instantiation

Only one input buffer is required to be instantiated in the design and placed on the correct IO_L#P location. The N-side of the buffer will be reserved and no other IOB will be allowed to be placed on this location. In the physical device, a configuration option is enabled that routes the pad wire from the IO_L#N IOB to the differential input buffer located in the IO_L#P IOB. The output of this buffer then drives the output of the IO_L#P cell or the input register in the IO_L#P IOB. In EPIC it will appear that the second buffer is unused. Any attempt to use this location for another purpose will cause a DRC error from the software.

**VHDL instantiation**

```
data0_p : IBUF_LVDS port map (I=>data(0), O=>data_int(0));
```

**Verilog instantiation**

```
IBUF_LVDS data0_p (.I(data[0]), .O(data_int[0]));
```

## Location constraints

All LVDS buffers must be explicitly placed on a device. For the input buffers this may be done with the following constraint in the .ucf or .ncf file.

```
NET data<0> LOC = D28; # IO_L0P
```

## Optional N-side

Some designers may prefer to also instantiate the N-side buffer for the input buffer. This will allow the top-level netlist to include both net connections for PCB layout and system level integration. In this case the output P-side IBUF connection is the only one to have a net connected to it. Since the N-side IBUF does not have a connection in the EDIF netlist it will be trimmed from the design in MAP.

### VHDL instantiation

```
data0_p : IBUF_LVDS port map (I=>data_p(0), O=>data_int(0));
data0_n : IBUF_LVDS port map (I=>data_n(0), O=>open);
```

### Verilog instantiation

```
IBUF_LVDS data0_p (.I(data_p[0]), .O(data_int[0]));
IBUF_LVDS data0_n (.I(data_n[0]), .O());
```

## Location constraints

All LVDS buffers must be explicitly placed on a device. For the global clock input buffers this may be done with the following constraint in the .ucf or .ncf file.

```
NET data_p<0> LOC = D28; # IO_L0P
NET data_n<0> LOC = B29; # IO_L0N
```

## Adding a Input Register

All LVDS buffers may have an input register in the IOB. The input register will be in the P-side IOB only. All the normal IOB register options are available (FD, FDE, FDC, FDCE, FDP, FDPE, FDR, FDRE, FDS, FDSE, LD, LDE, LDC, LDCE, LDP, LDPE). The register elements may be inferred or explicitly instantiated in the HDL code.

The register elements may be packed in the IOB using the IOB property to TRUE on the register or by using the "`map -pr [i|o|b]`" where "i" is inputs only, "o" is outputs only and "b" is both inputs and outputs.

To improve design coding times VHDL and Verilog synthesis macro libraries available to explicitly create these structures. The input library macros are listed in Table 28. The I and IB inputs to the macros are the external net connections.

**Table 28: Input Library Macros**

| Name | Inputs | Outputs |
|---|---|---|
| IBUFDS_FD_LVDS | I, IB, C | Q |
| IBUFDS_FDE_LVDS | I, IB, CE, C | Q |
| IBUFDS_FDC_LVDS | I, IB, C, CLR | Q |
| IBUFDS_FDCE_LVDS | I, IB, CE, C, CLR | Q |
| IBUFDS_FDP_LVDS | I, IB, C, PRE | Q |
| IBUFDS_FDPE_LVDS | I, IB, CE, C, PRE | Q |
| IBUFDS_FDR_LVDS | I, IB, C, R | Q |
| IBUFDS_FDRE_LVDS | I, IB, CE, C, R | Q |
| IBUFDS_FDS_LVDS | I, IB, C, S | Q |
| IBUFDS_FDSE_LVDS | I, IB, CE, C, S | Q |
| IBUFDS_LD_LVDS | I, IB, G | Q |
| IBUFDS_LDE_LVDS | I, IB, GE, G | Q |
| IBUFDS_LDC_LVDS | I, IB, G, CLR | Q |
| IBUFDS_LDCE_LVDS | I, IB, GE, G, CLR | Q |
| IBUFDS_LDP_LVDS | I, IB, G, PRE | Q |
| IBUFDS_LDPE_LVDS | I, IB, GE, G, PRE | Q |

## Creating a LVDS Output Buffer

LVDS output buffer may be placed in wide number of IOB locations. The exact location are dependent on the package that is used. The Virtex-E package information lists the possible locations as IO_L#P for the P-side and IO_L#N for the N-side where # is the pair number.

### HDL Instantiation

Both output buffer are required to be instantiated in the design and placed on the correct IO_L#P and IO_L#N locations. The IOB must have the same net source the following pins, clock (C), set/reset (SR), output (O), output clock enable (OCE). In addition, the output (O) pins must be inverted with respect to each other and if output registers are used the INIT states must be opposite values (one HIGH and one LOW). Failure to follow these rules will lead to DRC errors in software.

**VHDL instantiation**

```
data0_p  : OBUF_LVDS port map (I=>data_int(0),   O=>data_p(0));
data0_inv: INV       port map (I=>data_int(0),   O=>data_n_int(0));
data0_n  : OBUF_LVDS port map (I=>data_n_int(0), O=>data_n(0));
```

**Verilog instantiation**

```
OBUF_LVDS data0_p   (.I(data_int[0]),   .O(data_p[0]));
INV       data0_inv (.I(data_int[0],    .O(data_n_int[0]);
OBUF_LVDS data0_n   (.I(data_n_int[0]), .O(data_n[0]));
```

### Location constraints

All LVDS buffers must be explicitly placed on a device. For the output buffers this may be done with the following constraint in the .ucf or .ncf file.

```
NET data_p<0> LOC = D28; # IO_L0P
NET data_n<0> LOC = B29; # IO_L0N
```

## Synchronous vs. Asynchronous Outputs

If the outputs are synchronous (registered in the IOB) then any IO_L#P|N pair may be used. If the output are asynchronous (no output register) then they must use one of pairs that part of the same IOB group at the end of a ROW or COLUMN in the device.

The LVDS pairs that may be used as asynchronous outputs are listed in the Virtex-E pinout tables. Some pairs are marked as asynchronous capable for all devices in that package and others are marked as only available for that device in the package. If the device size may be changed at some point in the product lifetime then only the common pairs for all packages should be used.

## Adding an Output Register

All LVDS buffers may have an output register in the IOB. The output registers must be in both the P-side and N-side IOBs. All the normal IOB register options are available (FD, FDE, FDC, FDCE, FDP, FDPE, FDR, FDRE, FDS, FDSE, LD, LDE, LDC, LDCE, LDP, LDPE). The register elements may be inferred or explicitly instantiated in the HDL code.

Special care must be taken to insure that the D pins of the registers are inverted and that the INIT states of the registers are opposite. The clock pin (C), clock enable (CE) and set/reset (CLR/PRE or S/R) pins must connect to the same source. Failure to do this will lead to a DRC error in the software.

The register elements may be packed in the IOB using the IOB property to TRUE on the register or by using the "map -pr [i|o|b]" where "i" is inputs only, "o" is outputs only and "b" is both inputs and outputs.

To improve design coding times VHDL and Verilog synthesis macro libraries have been developed to explicitly create these structures. The output library macros are listed in Table 29. The O and OB inputs to the macros are the external net connections.

**Table 29: Output Library Macros**

| Name | Inputs | Outputs |
|---|---|---|
| OBUFDS_FD_LVDS | D, C | O, OB |
| OBUFDS_FDE_LVDS | DD, CE, C | O, OB |
| OBUFDS_FDC_LVDS | D, C, CLR | O, OB |
| OBUFDS_FDCE_LVDS | D, CE, C, CLR | O, OB |
| OBUFDS_FDP_LVDS | D, C, PRE | O, OB |
| OBUFDS_FDPE_LVDS | D, CE, C, PRE | O, OB |
| OBUFDS_FDR_LVDS | D, C, R | O, OB |
| OBUFDS_FDRE_LVDS | D, CE, C, R | O, OB |
| OBUFDS_FDS_LVDS | D, C, S | O, OB |
| OBUFDS_FDSE_LVDS | D, CE, C, S | O, OB |
| OBUFDS_LD_LVDS | D, G | O, OB |
| OBUFDS_LDE_LVDS | D, GE, G | O, OB |
| OBUFDS_LDC_LVDS | D, G, CLR | O, OB |
| OBUFDS_LDCE_LVDS | D, GE, G, CLR | O, OB |
| OBUFDS_LDP_LVDS | D, G, PRE | O, OB |
| OBUFDS_LDPE_LVDS | D, GE, G, PRE | O, OB |

## Creating a LVDS Output 3-State Buffer

LVDS output 3-state buffer may be placed in wide number of IOB locations. The exact location are dependent on the package that is used. The Virtex-E package information lists the possible locations as IO_L#P for the P-side and IO_L#N for the N-side where # is the pair number.

### HDL Instantiation

Both output 3-state buffer are required to be instantiated in the design and placed on the correct IO_L#P and IO_L#N locations. The IOB must have the same net source the following pins, clock (C), set/reset (SR), 3-state (T), 3-state clock enable (TCE), output (O), output clock enable (OCE). In addition, the output (O) pins must be inverted with respect to each other and if output registers are used the INIT states must be opposite values (one High and one Low). If 3-state registers are used the must be initialized to the same state. Failure to follow these rules will lead to DRC errors in the software.

**VHDL instantiation**

```
data0_p:   OBUFT_LVDS port map (I=>data_int(0), T=>data_tri,
O=>data_p(0));
data0_inv: INV port map     (I=>data_int(0), O=>data_n_int(0));
data0_n:    OBUFT_LVDS port map (I=>data_n_int(0), T=>data_tri,
O=>data_n(0));
```

**Verilog instantiation**

```
OBUFT_LVDS data0_p (.I(data_int[0]), .T(data_tri),O(data_p[0]));
INV        data0_inv(.I(data_int[0], .O(data_n_int[0]);
OBUFT_LVDS data0_n (.I(data_n_int[0]),.T(data_tri),.O(data_n[0]));
```

### Location constraints

All LVDS buffers must be explicitly placed on a device. For the output buffers this may be done with the following constraint in the .ucf or .ncf file.

```
NET data_p<0> LOC = D28; # IO_L0P
NET data_n<0> LOC = B29; # IO_L0N
```

### Synchronous vs. Asynchronous 3-State Outputs

If the outputs are synchronous (registered in the IOB) then any IO_L#P|N pair may be used. If the outputs are asynchronous (no output register) then they must use one of pairs that part of the same IOB group at the end of a ROW or COLUMN in the device. This applies for either the 3-state pin or the data out pin.

The LVDS pairs that may be used as asynchronous outputs are listed in the Virtex-E pinout tables. Some pairs are marked as asynchronous capable for all devices in that package and others are marked as only available for that device in the package. If the device size may be changed at some point in the product lifetime then only the common pairs for all packages should be used.

### Adding Output and 3-state Registers

All LVDS buffers may have an output register in the IOB. The output registers must be in both the P-side and N-side IOBs. All the normal IOB register options are available (FD, FDE, FDC, FDCE, FDP, FDPE, FDR, FDRE, FDS, FDSE, LD, LDE, LDC, LDCE, LDP, LDPE). The register elements may be inferred or explicitly instantiated in the HDL code.

Special care must be taken to insure that the D pins of the registers are inverted and that the INIT states of the registers are opposite. The 3-state (T), 3-state clock enable (CE), clock pin (C), output clock enable (CE) and set/reset (CLR/PRE or S/R) pins must connect to the same source. Failure to do this will lead to a DRC error in the software.

The register elements may be packed in the IOB using the IOB property to TRUE on the register or by using the "`map -pr [i|o|b]`" where "i" is inputs only, "o" is outputs only and "b" is both inputs and outputs.

To improve design coding times VHDL and Verilog synthesis macro libraries have been developed to explicitly create these structures. The input library macros are listed below. The 3-state is configured to be 3-stated at GSR and when the PRE,CLR,S or R is asserted and shares it's clock enable with the output register. If this is not desirable then the library may be updated be the user for the desired functionality. The O and OB inputs to the macros are the external net connections.

## Creating a LVDS Bidirectional Buffer

LVDS bidirectional buffer may be placed in wide number of IOB locations. The exact location are dependent on the package that is used. The Virtex-E package information lists the possible locations as IO_L#P for the P-side and IO_L#N for the N-side where # is the pair number.

### HDL Instantiation

Both bidirectional buffer are required to be instantiated in the design and placed on the correct IO_L#P and IO_L#N locations. The IOB must have the same net source the following pins, clock (C), set/reset (SR), 3-state (T), 3-state clock enable (TCE), output (O), output clock enable (OCE). In addition, the output (O) pins must be inverted with respect to each other and if output registers are used the INIT states must be opposite values (one HIGH and one LOW). If 3-state registers are used the must be initialized to the same state. Failure to follow these rules will lead to DRC errors in the software.

**VHDL instantiation**

```
data0_p:   IOBUF_LVDS port map (I=>data_out(0), T=>data_tri,
IO=>data_p(0), O=>data_int(0));
data0_inv: INV       port map (I=>data_out(0),   O=>data_n_out(0));
data0_n  : IOBUF_LVDS port map (I=>data_n_out(0), T=>data_tri,
IO=>data_n(0), O=>open);
```

**Verilog instantiation**

```
IOBUF_LVDS data0_p(.I(data_out[0]), .T(data_tri), .IO(data_p[0]),
.O(data_int[0]);
INV        data0_inv (.I(data_out[0],    .O(data_n_out[0]);
IOBUF_LVDS data0_n (.I(data_n_out[0]), .T(data_tri),
.IO(data_n[0]).O());
```

### Location constraints

All LVDS buffers must be explicitly placed on a device. For the output buffers this may be done with the following constraint in the .ucf or .ncf file.

```
NET data_p<0> LOC = D28; # IO_L0P
NET data_n<0> LOC = B29; # IO_L0N
```

## Synchronous vs. Asynchronous Bidirectional Buffers

If the output side of the bidirectional buffers are synchronous (registered in the IOB) then any IO_L#P|N pair may be used. If the output side of the bidirectional buffers are asynchronous (no output register) then they must use one of pairs that part of the same IOB group at the end of a ROW or COLUMN in the device. This applies for either the 3-state pin or the data out pin.

The LVDS pairs that may be used as asynchronous bidirectional buffers are listed in the Virtex-E pinout tables. Some pairs are marked as asynchronous capable for all devices in that package and others are marked as only available for that device in the package. If the device size may be changed at some point in the product lifetime then only the common pairs for all packages should be used.

## Adding Output and 3-state Registers

All LVDS buffers may have an output and input registers in the IOB. The output registers must be in both the P-side and N-side IOBs, the input register is only in the P-side. All the normal IOB register options are available (FD, FDE, FDC, FDCE, FDP, FDPE, FDR, FDRE, FDS, FDSE, LD, LDE, LDC, LDCE, LDP, LDPE). The register elements may be inferred or explicitly instantiated in the HDL code. Special care must be taken to insure that the D pins of the registers are inverted and that the INIT states of the registers are opposite. The 3-state (T), 3-state clock enable (CE), clock pin (C), output clock enable (CE) and set/reset (CLR/PRE or S/R) pins must connect to the same source. Failure to do this will lead to a DRC error in the software.

The register elements may be packed in the IOB using the IOB property to TRUE on the register or by using the "`map -pr [i|o|b]`" where "i" is inputs only, "o" is outputs only and "b" is both inputs and outputs. To improve design coding times VHDL and Verilog synthesis macro libraries have been developed to explicitly create these structures. The bidirectional I/O library macros are listed in Table 30. The 3-state is configured to be 3-stated at GSR and when the PRE, CLR, S or R is asserted and shares it's clock enable with the output and input register. If this is not desirable then the library may be updated be the user for the desired functionality. The IO and IOB inputs to the macros are the external net connections.

**Table 30: Bidirectional I/O Library Macros**

| Name | Inputs | Bidirectional | Outputs |
|---|---|---|---|
| IOBUFDS_FD_LVDS | D, T, C | IO, IOB | Q |
| IOBUFDS_FDE_LVDS | D, T, CE, C | IO, IOB | Q |
| IOBUFDS_FDC_LVDS | D, T, C, CLR | IO, IOB | Q |
| IOBUFDS_FDCE_LVDS | D, T, CE, C, CLR | IO, IOB | Q |
| IOBUFDS_FDP_LVDS | D, T, C, PRE | IO, IOB | Q |
| IOBUFDS_FDPE_LVDS | D, T, CE, C, PRE | IO, IOB | Q |
| IOBUFDS_FDR_LVDS | D, T, C, R | IO, IOB | Q |
| IOBUFDS_FDRE_LVDS | D, T, CE, C, R | IO, IOB | Q |
| IOBUFDS_FDS_LVDS | D, T, C, S | IO, IOB | Q |
| IOBUFDS_FDSE_LVDS | D, T, CE, C, S | IO, IOB | Q |
| IOBUFDS_LD_LVDS | D, T, G | IO, IOB | Q |
| IOBUFDS_LDE_LVDS | D, T, GE, G | IO, IOB | Q |
| IOBUFDS_LDC_LVDS | D, T, G, CLR | IO, IOB | Q |
| IOBUFDS_LDCE_LVDS | D, T, GE, G, CLR | IO, IOB | Q |
| IOBUFDS_LDP_LVDS | D, T, G, PRE | IO, IOB | Q |
| IOBUFDS_LDPE_LVDS | D, T, GE, G, PRE | IO, IOB | Q |

## Revision History

| Date | Version # | Revision |
|---|---|---|
| 08.09.99 | 1.0 | Initial release. |
| 10.21.98 | 1.11 | Updated |
| 10.11.99 | 1.2 | Updated Table 4 & 5 to add packages. Corrected overall style, Updated for Virtex-E |
| 1.11.99 | 2.0 | Added Appendix A & B |
| 1.19.00 | 2.1 | Revised Figure 15 & 16, and Table 25. |