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The LVDS I/O Standard

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Summary

This application note describes the LVDS I/O standard. LVDS provides higher noise immunity than single-ended techniques, allowing for higher transmission speeds, smaller signal swings, lower power consumption, and less electro-magnetic interference than single-ended signaling. Differential data can be transmitted at these rates using inexpensive connectors and cables. LVDS provides robust signaling for high-speed data transmission between chassis, boards, and peripherals using standard ribbon cables and IDC connectors with 100 mil header pins. Point-to-point LVDS signaling is possible at speeds of up to 622 Mb/s.

Introduction

Low-voltage differential signaling (LVDS) has emerged as a leading standard for differential signaling between boards, chassis and other peripherals. LVDS provides several benefits.

The Virtex™-E drivers and receivers provide several benefits:

- Direct board-to-board high-speed interface,
- Much higher signaling speeds than with single-ended interfaces,
- Better signal integrity due to source termination than with other LVDS drivers,
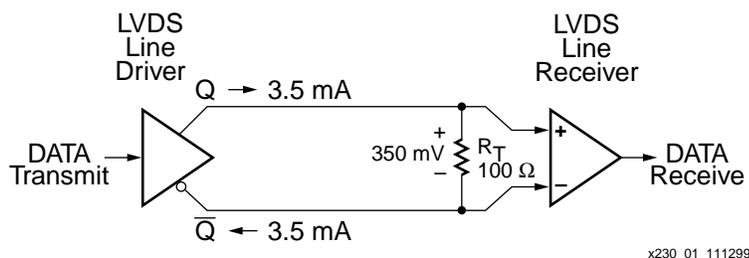- Reduced board area,
- Reduced signal delay/skew.

Figure 1: A Typical Point-to-Point LVDS Application

Standard LVDS DC Specifications

Figure 1 shows a typical point-to-point LVDS application. An LVDS driver on the left drives the two 50 Ω transmission lines into an LVDS receiver on the right. The Q and $\overline{Q}$ outputs of the LVDS driver pass to the corresponding inputs of the LVDS receiver. The two 50 Ω single-ended transmission lines can be microstrip, stripline, or a 100 Ω differential twisted pair or similar balanced differential transmission line. A 100 Ω resistor R_T terminates the Q and $\overline{Q}$ signals. LVDS uses a current-mode driver, behaving like two equal and opposite current sources with a high output impedance. LVDS outputs typically drive ±3.5 mA to flow through the 100 Ω resistor R_T generating a ±350 mV voltage swing (Q - $\overline{Q}$). The terms "common-mode voltage" and "offset voltage" refer to the average of Q and $\overline{Q}$, (Q +$\overline{Q}$)/2. LVDS has a typical output common-mode voltage of 1.25 V, determined by the LVDS driver. Table 1 summarizes the DC specifications of LVDS.

Figure 2 shows how to implement the 50 Ω lines using microstrip techniques on a PC board. Many combinations are possible, but these geometries allow for a compact 50 Ω line using standard 8-mil wide traces on the PC board. See Appendix A for a discussion of transmission lines and terminations used in LVDS. The 100 Ω termination resistor R_T terminates the LVDS_IN and $\overline{\text{LVDS\_IN}}$ nodes close to the Virtex-E device. The Virtex-E LVDS receiver, on the right in Figure 1, adheres to all the standard LVDS DC input levels specified in Table 1.

Table 1: Standard LVDS DC Specifications, V_{DD} = 2.5V

DC Parameter	Conditions	MIN	TYP	MAX	Units
Output High Voltage for Q and $\overline{Q}$	R_T = 100 Ω across Q and $\overline{Q}$ signals	-	1.38	1.6	V
Output Low Voltage for Q and $\overline{Q}$	R_T = 100 Ω across Q and $\overline{Q}$ signals	0.90	1.03	-	V
Differential Output Voltage (Q - $\overline{Q}$), Q = High ($\overline{Q}$ - Q), $\overline{Q}$ = High	R_T = 100 Ω across Q and $\overline{Q}$ signals	250	350	450	mV
Output Common-Mode Voltage (Q + $\overline{Q}$) / 2	R_T = 100 Ω across Q and $\overline{Q}$ signals	1.125	1.25	1.375	V
Differential Input Voltage (Q - $\overline{Q}$), Q = High ($\overline{Q}$ - Q), $\overline{Q}$ = High	Common-mode input voltage = 1.25 V	100	350	-	mV
Input Common-Mode Voltage (Q + $\overline{Q}$) / 2	Differential input voltage = ±350 mV	0.25	1.25	2.25	V
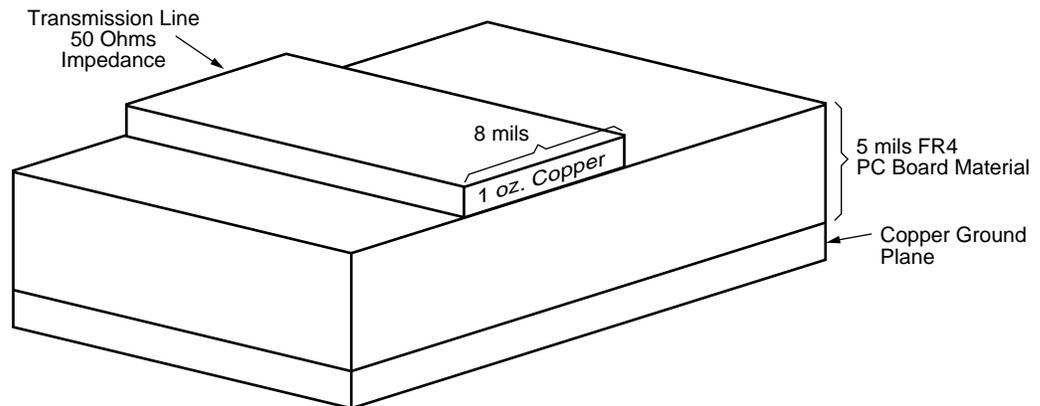
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Figure 2: A 50 Ω transmission line construction in microstrip.

Standard LVDS AC Performance

The LVDS circuit of Figure 1 provides a nearly ideal termination to the differential transmission lines. This termination permits the circuit to drive data at speeds of up to 622 Mb/s reliably. Figure 3 shows the resulting performance of such an LVDS circuit including package parasitics at 622 Mb/s. The response curves of Figure 3 were simulated using a SPICE model for generic LVDS drivers going into a 5 ns (30 inches typically) transmission line. This simulation included board and package parasitic capacitances and inductances on the driver and receiver devices. Data and clocks can be transmitted over longer cables exceeding 5 ns in electrical propagation delay, limited only by the quality of the cable, namely the cable attenuation caused by skin effect losses at high frequencies. For a treatment on skin effect losses see the following reference on transmission line scaling by Howard Johnson at
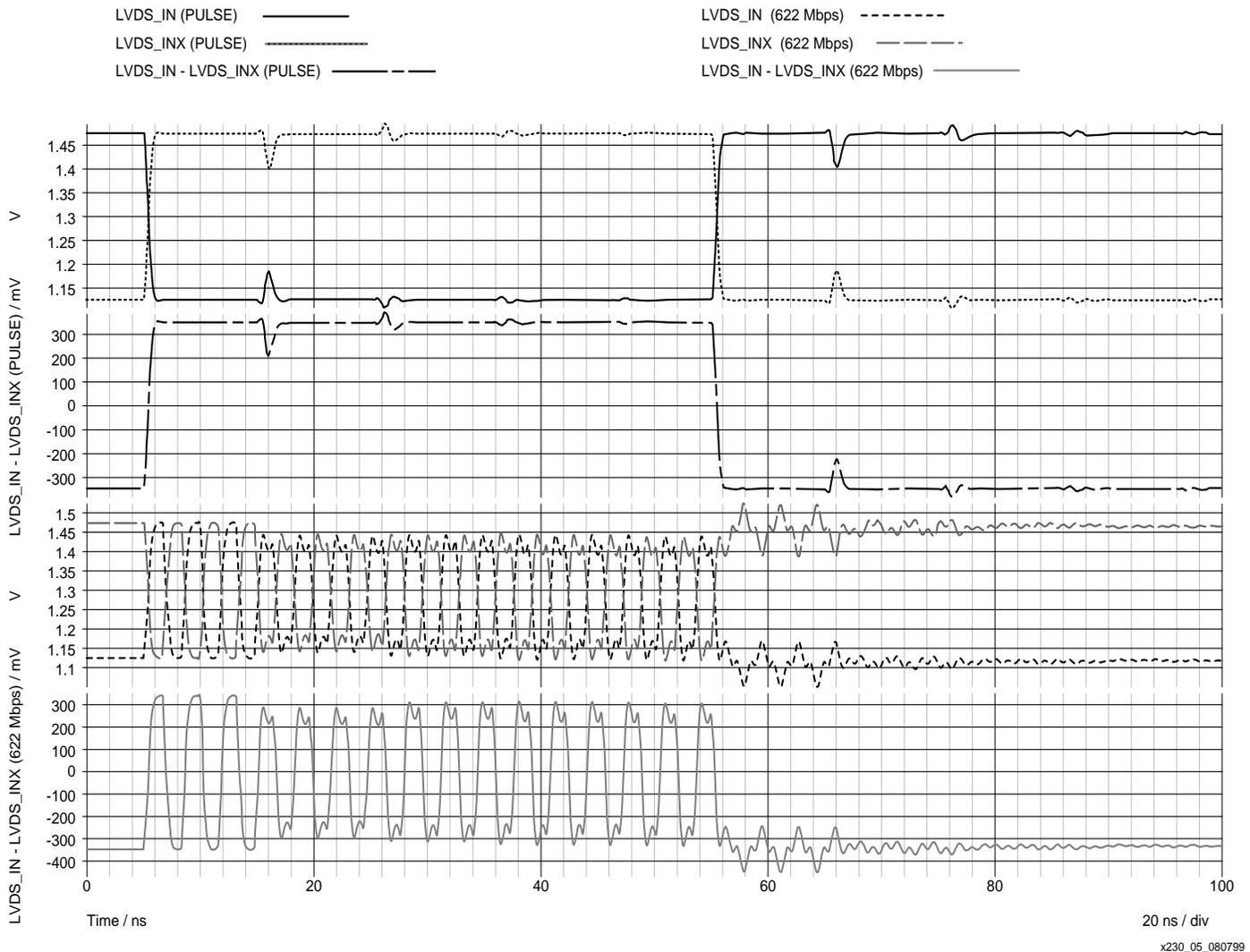
http://www.sigcon.com/articles/edn/tlinescaling.htm.

Figure 3: Typical LVDS Absolute and Difference Signals Showing Step and Burst Data Response at 622 Mb/s

PCB layout guidelines for Virtex-E LVDS

Printed-circuit board layout guidelines for the LVDS circuit in Figure 1 are as follows:

1. A multi-layer printed-circuit board with controlled transmission line impedances is required. Characteristic microstrip impedance guidelines are described in Table 1 of XAPP231.

2. All transmission lines between LVDS drivers and receivers should be referenced to a common ground plane except when routed through a balanced differential transmission line such as twisted-pair. For twisted-pair and other balanced lines, a grounded shield allows for common-mode return current. The shield should connect to the ground planes at the beginning and ending of the twisted-pair cable. If no shield connection is available, it is important to take extra care to use symmetric and equal-length routing. Balancing the capacitive load on the differential pair will reduce the conversion of common-mode noise to differential signal. The ground plane should have no breaks under the signal path to avoid large discontinuities from increased inductance.

3. Source termination resistors if any should lie close to the LVDS outputs for the LVDS line driver. The parallel termination resistor R_T needs to be close to the LVDS inputs at the destination.

4. The LVDS signal lines should have equal length with symmetric routing between source and destination to maximize common-mode rejection. The two LVDS signals should run close together on the PC board. If the trace spacing is less than the dielectric thickness to the ground plane, differential impedance effects must be included to determine the effective transmission line impedance since the trace impedance will be significantly affected by the differential impedance between the two traces. Wider spacings have a smaller effect on the impedance.

5. The differential LVDS output should use a pair of adjacent Virtex-E pins, preferably in the same output block of the Virtex-E FPGA (see FPGA_Editor plots for block clustering). The LVDS data must have a single clock driving both of the output IOBs to minimize output skew between the two pins.

Conclusion

LVDS provides a reliable signaling standard over cables, backplanes and on boards at data rates up to 622 Mb/s. Reliable data transmission is possible over electrical lengths exceeding 5 ns (30 inches), limited only by cable attenuation due to skin effect.

References

For a detailed discussion on the benefits of LVDS, including comprehensive system analyses, please go to the National Semiconductor LVDS Owner's Manual and Design Guide, located at:

http://www.national.com/appinfo/lvds/lvdstotal.pdf.

Texas Instruments has provided an overview of LVDS Technology Titled "Low Voltage Differential Signalling (LVDS) Technology: The Basics." The text of this article can be found online at:

http://www.ti.com/sc/docs/news/1998/98068b.htm

Texas Instruments has also measured the performance of various CAT5 cables for transporting LVDS differential signals:

http://www-s.ti.com/sc/psheets/slla053/slla053.pdf

Appendix A

Transmission Lines used in LVDS

LVDS is typically used to route data and clocks between boards, chassis, and peripherals. Since the transition times of LVDS signals are typically 500 ps, all circuit traces over 80 ps (1/6 of 500 ps) in electrical length must be treated as transmission lines. Assuming an FR4 PCB (printed-circuit board) transmission line has a propagation delay of 165 ps/inch, a 1/2-inch trace must be considered a transmission line when transmitting LVDS.
There are two main types of transmission lines used in LVDS:

1. Signals referenced to ground, i.e. coaxial cable, microstrip or stripline on PCB's

2. Balanced differential, without a physical ground plane i.e. twisted-pair.

Balanced refers to the axial symmetry of the differential transmission line. Single-ended transmission lines are referenced to a physical ground plane while balanced differential transmission lines are referenced to an imaginary virtual ground called an image plane. The image plane is formed, by symmetry, when the physical layout of two traces or wires is symmetrical along the entire length of the connection and the signals propagating along the two wires are equal and opposite in magnitude. The surface of symmetry between the wires or traces becomes the image plane since the fields cancel in that region. The image plane for a ribbon cable is a plane halfway between two conductors, perpendicular to the plane of the ribbon cable. The image plane for a twisted-pair is a twisted plane halfway between conductors.

The image plane can be treated as a ground plane when making transmission line calculations. For example, a twisted-pair transmission line that has a 100 Ω characteristic impedance has an equivalent single-ended characteristic impedance of 50 Ω when the signals propagating are differential. Therefore, a 100 Ω twisted-pair transmission line propagating a differential signal has exactly the same characteristics (except for propagation delay, 135 ps/inch) as two 50 Ω microstrips or striplines on a PCB propagating a differential signal.

Using this concept, LVDS interconnected with dual 50 Ω microstrip/striplines and a single 100 Ω twisted pair can be reduced to two 50 Ω single-ended transmission line equivalents for the entire length of the connection. The image plane cuts the parallel termination resistor R_T in half and the resulting $R_T/2 = 50\ \Omega$ resistor parallel terminates the single-ended equivalent 50 Ω transmission line.

So far, only the differential mode of propagation has been considered. An equally important and often neglected mode is common-mode propagation, whereby the same polarity signal propagates down both lines simultaneously. Understanding common-mode propagation is especially important for balanced differential transmission lines such as twisted-pairs. Two arbitrary signals can always be reduced to their differential and common-mode components. In contrast to differential mode where the signals are equal in magnitude and opposite in sign, common-mode signals have exactly the same magnitude and sign at all times. When a common-mode signal travels down a single-ended transmission line like a microstrip, the propagation behavior is exactly the same as differential signal propagation since a physical ground plane exists. However, when a common-mode signal travels down a balanced differential transmission line like a twisted-pair, the propagation behavior can be dramatically different than the differential propagation since there is no image plane or physical ground plane for fields to terminate. Since the common-mode signal is identical in both wires, the current is also the same. By Kirchoff's Current Law, the equal currents that flow down the two wires must somehow return. Typically, the return current flows through a third wire called a shield. If there is no shield, then the common-mode return current must find a longer more circuitous path to return (sometimes through the power supplies). This will cause common-mode inductance to increase substantially. When common-mode inductance increases, common-mode voltages induced by common-mode currents increase causing intermittent data errors due to common-mode to differential mode conversion (from mismatches between the signal paths). Therefore, use a shield connection or wire attached to the source and destination ground to minimize common-mode impedance at high frequencies. Ideally, the shield connects

at the points where the microstrips and/or striplines attach to the twisted-pair and routes parallel to the twisted-pair, since the shortest return path is next to the twisted-pair.

Revision History

Date	Version #	Revision
10.1.99	1.0	Initial Xilinx release.
11.16.99	1.1	Minor revisions and the addition of a Reference Section