THE NEW Virtex-E

3.2-Million Gate, *High-bandwidth* FPGA Family

With up to 622 MHz differential I/O performance, Virtex-E FPGAs are the high-bandwidth solution for your next generation high performance systems.

by Bruce Jorgens, Virtex Product Marketing Manager, Xilinx, jorgens@xilinx.com

The new Virtex-E FPGA family is built on the highly successful Virtex architecture. Leveraging our latest 0.18-micron, six-layer metal technology, Virtex-E devices now give you up to 3.2 million system gates, 804 I/Os, and up to 622 MHz differential I/O performance. Combined with system-level features for clock management, multiple I/O standards, and embedded True Dual-Port™ memory, the Virtex-E family is designed to support the high bandwidth requirements of next generation high performance DSP and communication systems.

Device	Logic Cells	Dual-Port Block Memory (Kbits)	Maximum User I/O	I/O Bandwidth (Gbits/sec)
XCV50E	1728	56	176	44
XCV100E	2700	80	176	44
XCV200E	5292	112	284	71
XCV300E	6912	128	316	79
XCV400E	10800	160	404	100
XCV600E	15552	288	512	127
XCV1000E	27648	384	660	164
XCV1600E	34992	576	724	180
XCV2000E	43200	640	804	200
XCV2600E	57132	736	804	200
XCV3200E	73008	832	804	200

1 I/O bandwidth = (80% max. user I/O) x (311 Mbps)

Table 1 - Virtex-E Features

Many designs will require multiple high bandwidth data ports with I/O bandwidth distributed across the required ports as shown in Table 1. Virtex-E devices range from 44 Gbps to 200 Gbps I/O bandwidth. For applications such as OC-192, Virtex-E devices can easily support the multiple 10-Gbps data ports that are required.

Bandwidth-enabling Technology

The Virtex-E devices contain advanced system-level technology that is specifically designed to support high bandwidth applications. Figure 1 shows a block diagram of the Virtex-E bandwidth-enabling technology including digital Delay Lock Loops (DLLs), True Dual-Port embedded memory, and SelectI/O+ technology.

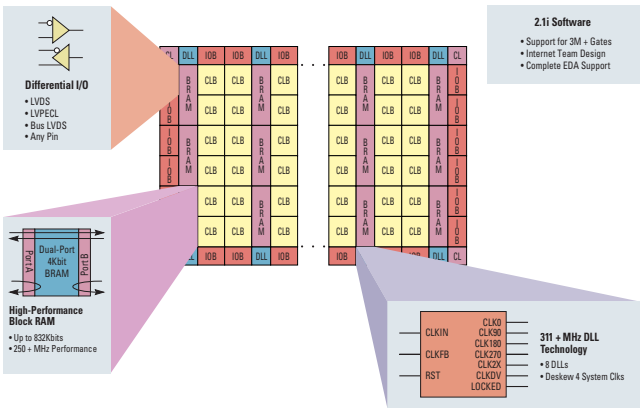


Figure 1 - Virtex-E Architecture Overview

Eight High Performance DLLs

The Virtex-E advanced DLL technology provides the system clock management that is necessary for high bandwidth chip-to-chip or backplane applications. The DLL circuitry allows very precise synchronization of external and internal clocks. Xilinx was the first to deliver this technology by offering four 200 MHz DLLs in each Virtex device. The Virtex-E family takes this technology to the next level offering eight DLLs in each Virtex-E device.

As a fully digital implementation, the Virtex and Virtex-E DLLs do not have the typical problems encountered with analog phase locked loops (PLLs); PLLs are extremely sensitive to noise on the power and ground pins. Many systems cannot provide the isolation and decoupling required for the proper operation of a PLL, while the Virtex-E DLLs have no special requirements. Also, because the DLL is not sensitive to process variations, it is offered as a standard feature in every device, and every speed grade.

Virtex-E DLLs provide precise clock edges through phase shifting, frequency multiplication, and frequency division. Table 2 shows the basic characteristics of the Virtex-E DLLs.

Parameter	Value
Maximum Output Frequency	320 MHz*
Maximum Output Jitter	100 ps
Output Frequency Duty Cycle	50%+/- 100ps

* Based on Virtex-E –7speed grade product

Table 2 - Bandwidth-critical Specifications of the Virtex-E DLL

Maximizing Memory Bandwidth with Virtex-E DLLs

A key technique for increasing the bandwidth of a particular data port is to have signals change on both edges of the clock, commonly referred to as the "Double Data Rate" technique. At high frequencies, signal integrity limits the clock performance, which limits the bandwidth of the data. Bandwidth for the port is immediately doubled if the architecture can change data at each edge of a system clock. Memory suppliers have already started to support this type of high performance technique to increase the memory bandwidth of their devices.

For this technique to work, it is critical that the clock duty cycle be as close to 50 percent as possible. Because Virtex-E DLLs can generate clocks with a duty cycle guaranteed to be within 100 picoseconds of 50 percent, you can achieve the maximum memory bandwidth when interfacing to the fastest DDR memories. Figure 2 demonstrates how Virtex-E DLLs, coupled with the SelectI/O+™ technology, help achieve maximum bandwidth in a 266MHz DDR application.

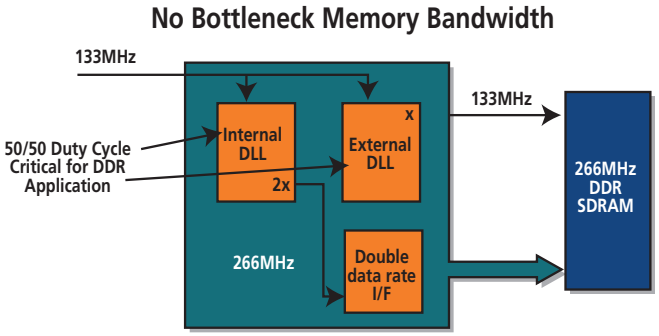


Figure 2 - Virtex-E Interfacing to a 266 MHz DDR SDRAM Memory

SelectI/O+ Technology

To meet high bandwidth requirements, electrical signals must switch at over 100 MHz; standard TTL and CMOS signal technology cannot keep pace. With the original Virtex family, Xilinx pioneered the SelectI/O™ technology which supports 200 MHz I/O and allows a single FPGA to interface with any other device without external converters. Virtex-E SelectI/O+ technology expands the performance and flexibility by supporting high performance I/O standards such as HSTL and SSTL at over 300 Megabits per second (Mbps) per pin. In addition, Virtex-E devices are the first programmable logic devices to directly interface with differential I/O standards including LVDS, Bus LVDS (BLVDS), and LVPECL.

Standard	Typical Application
LVTTL	3.3 V General Purpose
LVCMOS2	2.5 V General Purpose
LVCMOS18	1.8 V General Purpose
PCI33_3	33 MHz 3.3 V PCI Backplane
PCI66_3	66 MHz 3.3 V PCI Backplane
SSTL2 (I,II), SSTL3(I,II), CTT	SDRAM, DDR SRAM
HSTL(I,III,IV)	SRAM, DDR SDRAM, Backplanes
GTL, GTL+, AGP	Backplanes, Microprocessor Interfacing
LVDS	Point to Point and Multi-drop Backplanes High Noise Immunity
BLVDS	Bus LVDS Backplanes, High Noise Immunity, Bus Architecture Backplanes
LVPECL	High Performance Clocking, Backplanes, Differential 100MHz+ Clocking, Optical Transceiver, High Speed Networking, and Mixed-Signal Interfacing
5 V TTL* (4mA Iol)	Legacy 5V TTL Interfacing

*Requires 100 Ohms external resistor

Table 3 - I/O standards Supported by Virtex-E Family

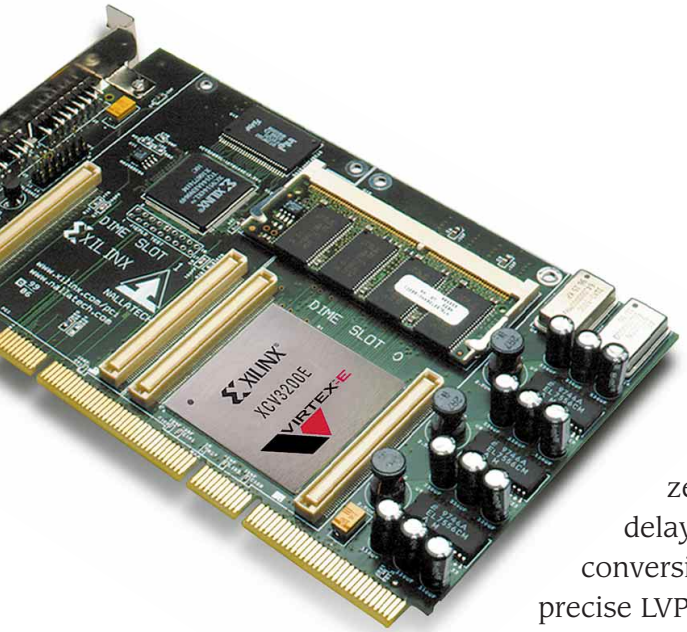
High-performance Differential Signaling: LVPECL, LVDS, and Bus LVDS

Increasingly, leading systems designers are turning to differential signaling as the mechanism of choice for backplane applications. Differential signaling enables high bandwidth while reducing power, increasing noise immunity, and decreasing EMI emissions. Virtex-E devices meet this emerging challenge with unprecedented capabilities and support for high-performance differential signaling.

The Virtex-E family supports a hierarchy of differential solutions including up to 36 pairs of LVDS and/or LVPECL operating at 622 MHz, and up to 344 differential pairs operating up to 311 MHz. This gives you a maximum differential I/O bandwidth of over 100 Gbps, which can be distributed over the three differential signal standards as needed. For the first time in a programmable device, you can leverage the high bandwidth and noise immunity characteristics of these standards.

LVPECL I/O is widely used in 100+ MHz inter-chip signaling in high-speed data communications and instrumentation systems. Fiber-optic network interfaces and gigahertz analog-to-digital converters, for example, rely on LVPECL I/O to achieve gigabit per second bandwidth. All Virtex-E differential I/Os support LVPECL input, output, and I/O signaling.

In addition to high-speed interfacing, LVPECL is the industry standard for transmission of precise, on-board clocks at frequencies in excess of 100 MHz. While traditional LVTTL clock sources are typically limited to 100 MHz and below (due to the fundamental signal integrity limits), LVPECL clock sources provide operation up to 400 MHz. As FPGA system clock frequencies exceed 100 MHz, LVPECL clocking becomes an essential requirement. Virtex-E devices support high-performance LVPECL clock inputs for global and local clocking, with frequencies in excess of 300 MHz. In addition, through the use of its multiple DLLs coupled with SelectI/O+ technology, the Virtex-E devices



enable zero-delay conversion of precise LVPECL clocks into any required I/O standard. Thus, Virtex-E FPGAs are an integral part of high-performance board-level clock distribution strategies.

In addition to LVPECL, the Virtex-E family has the industry's first programmable devices to support Low-Voltage Differential Signaling (LVDS). LVDS exists in two commonly available variants: LVDS and Bus LVDS. LVDS is optimized for high-speed point-to-point links, while Bus LVDS is optimized for backplane applications employing multi-drop (one transmitter, multiple receiver), and multi-point (multiple transmitters and receivers) configurations.

Virtex-E devices provide unparalleled support for both LVDS and Bus LVDS, with support on all devices and speed grades. You can use up to 688 pins (344 pairs) of LVDS and Bus LVDS capabilities on the largest device, providing differential I/O bandwidth in excess of 100 Gbps.

True Dual-Port Embedded Block Memory

Whether used as FIFOs, caches, or ATM packet buffers, the system requirements for more memory grows much faster than logic requirements. Xilinx pioneered using embedded distributed memory (with its SelectRAM technology) in its XC4000 FPGAs, allowing the configurable logic block to support logic or memory. With the Virtex series, this technology was enhanced to include up to 128 Kbits of True Dual-Port block RAM. The Virtex-E family again provides a quantum leap in internal memory bandwidth by supporting up to 832 Kbits of True Dual-Port RAM (208 blocks of 4Kbits memory) capable of 250 MHz performance.

To emulate most of the functionality of a dual-port memory, two-port memory architectures require twice the number of memory bits and multiplexing of address and data as shown in Figure 3. This results in two-port memory at roughly half the bandwidth and half the efficiency of the Virtex-E True Dual-Port memory in any given configuration.

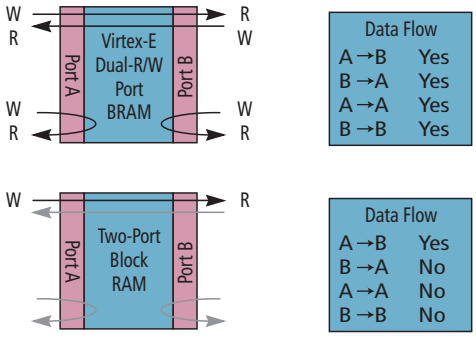


Figure 3 - Typical Memory Configurations

Managing Bandwidth Using True Dual-Port Memory

Each Virtex-E True Dual-Port memory block supports 4 Kbits of memory, and each port can be configured separately to support a variety of depth/width combinations. Embedded memory can buffer high bandwidth data as well as reduce the internal processing speed by transparently converting from one data width to another.

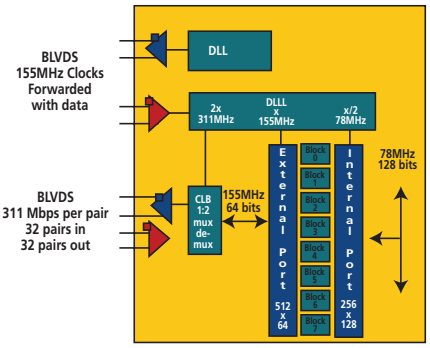


Figure 4 - An OC-192 Application Example

Figure 4 demonstrates an OC-192 application example. A data port with OC-192 bandwidth comes in on 32 BLVDS pairs running at 311 Mbps per pair. Eight blocks of embedded RAM are used to buffer the data internally. The port taking data from the I/O register to the memory is configured as 512 rows deep by 64 bits wide. The port leading to the internal processing of the data is configured as 256 by 128. Internal processing of the 128-bit data need only run at 78 MHz to keep up with the OC-192 bandwidth. An outgoing port would be configured similarly.

Packaging

To support a 10-Gbps bandwidth, the device package must be capable of packing many high performance I/Os in limited board space. The package must also be able to dissipate several watts of power. Virtex-E devices continue the tradition of offering the industry's most reliable and flexible packaging, including

- PQFP - Plastic quad flat pack.
- BGA - 1.27 mm ball grid array.
- CSP - Leading-edge 0.8 mm chip scale package.
- FG - 1.0 mm fine pitch BGA.

These packages are supported across the family.

For the fine pitch 1.0 mm BGA offering, the Virtex-E family introduces three new FG packages:

- FG900 - 31 mm X 31 mm.
- FG1156 - 35 mm X 35 mm.
- FG860 - 42.5 mm X 42.5 mm (thermally enhanced).

The Virtex-E family can now support up to 804 I/Os using board area as small as 35 mm by 35 mm. These packages set new standards in I/Os per square inch as well as maximum bandwidth per square inch.

Summary

The new Virtex-E FPGA family helps you meet the bandwidth requirements of the next generation high performance systems by giving you significant performance and flexibility enhancements in the areas of clock management, SelectI/O+ technology, True Dual-Port block memory, and high performance differential signaling.

For more detailed information on the Xilinx Virtex-E series, including data sheets and applications notes, visit the product section of the Xilinx website at www.xilinx.com.