CPLD ChipViewer - Graphical Design Control Made Simple

An interactive way to view and control your logic design routing within a Xilinx CPLD.

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ChipViewer™ is a powerful tool that allows you to see how your logic is implemented in a Xilinx CPLD. Its usefulness is realized at both the start and end of your design implementation.

In the Pre-fit mode, ChipViewer acts a graphical constraints entry tool, and allows you to pre-assign the pinout for your device. Your design I/O is displayed in a hierarchical form showing inputs, outputs, and global resources. With a simple mouse click you can assign I/O pinouts or prohibit pin usage. Package "thumbnails," which give you a top and bottom view, are also available to assist in intelligent logic and I/O placement. Macrocell register initial states, the power mode, and output slew rate values are also easily specified. Saving the modifications generates a user constraints file (*.ucf) which is used by the Xilinx fitting tool during implementation.

In the Post-fit mode, ChipViewer reads in the implemented design file and displays a representation of the logic placement within the device. Figure 1 illustrates the graphical features showing the color-coded interconnections that exist within the part. Clicking on an active macrocell shows either the inputs to the macrocell, the outputs from the macrocell, or both simultaneously. Double clicking on this same macrocell brings up an additional window that provides detailed information, such as the implemented equations along with a schematic representation of the logic that is contained in that macrocell.

Conclusion

ChipViewer allows you to intelligently interact with the logic in your Xilinx XC9500 CPLD designs, saving you time and making your job easier.

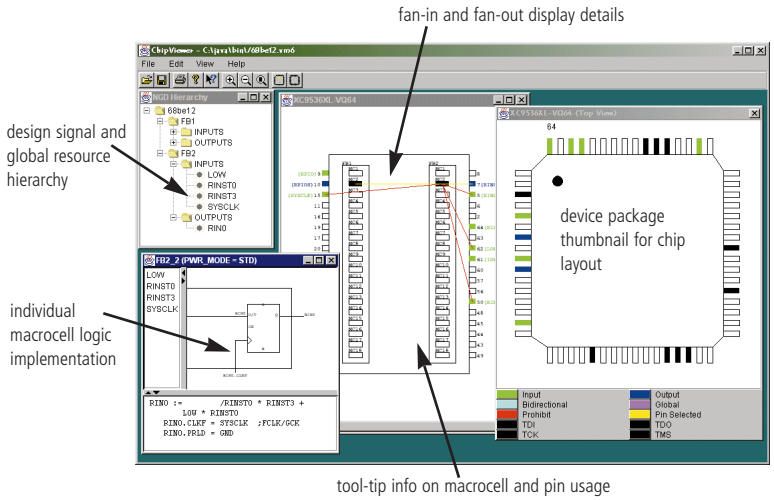

Figure 1 - CPLD Chip Viewer Capabilities

For more information see www.xilinx.com.