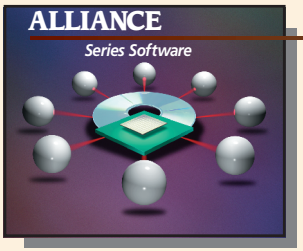
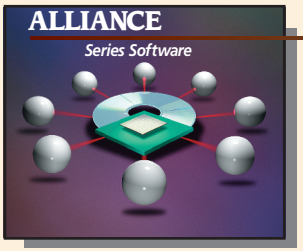


XILINX®

Synthesis • MTI
Implementation Flow

LogiBLOX
CORE Generator
.V
.VHD
.NGC= Xilinx Binary Netlist
NGC
VEI
VHI
VEO
VHO
Verilog & VHDL Instantiation
State Diagram Editor
Schematic Design Editor
HDL Editor
Renoir
VHDL Verilog
VHDL Verilog
EDIF
VHDL Verilog
VHDL Verilog
EDN
Functional Simulation Flow
Timing Requirements
CORE Generator
LogiBLOX
UNIFIED
Gates
UniSim
VITAL & Verilog
SimPrim
VITAL & Verilog
HDL Test Bench
Model Technology
MODELSIM
SIMULATOR
Timing Simulation Flow
VHDL Verilog
SDF
BIT JEDEC
Reports
Xilinx
IMPLEMENTATION
Tools
LEONARDO SPECTRUM
OR
3rd Party Synthesis
NCF
XNF EDIF
w/ Timing Constraints
VHDL Verilog
User Constraints File
Functional Simulation Flow
EG
PN 0010419 01



Model Technology (MTI) Information

Device Architecture Support

FPGA Product Family
- Spartan
- Virtex
- XC4000X

CPLD Product Family
- XC9500

About Model Technology

- VHDL, Verilog and Cosimulation of VHDL & Verilog

Full Language Support:
- VHDL IEEE-STD-1076 -'87, -'93
- Standard Logic IEEE-STD-1164
- VITAL IEEE-STD-1076.4 (VITAL)
- Verilog IEEE-STD-1364

Recommended Settings

For recommended settings, go to
http://www.xilinx.com
"Product" "Software Solutions"

Xilinx Contacts and Technical Support

World Wide Web:
http://www.xilinx.com

North America
1-800-255-7778
hotline@xilinx.com

France
33 1-3463-0100
frhelp@xilinx.com

United Kingdom
44 1932-820821
ukhelp@xilinx.com

Japan
81 3-3297-9163
jhotline@xilinx.com

Model Technology Contacts and Technical Support

World Wide Web:
http://www.model.com

Telephone
1-503-641-1340

E-Mail
support@model.com

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Guide Overview

1 Invoke the tools

PC Start→Programs→Model Tech→ModelSim

UNIX Separate programs
vlib, vmap, vcom, vlog, vsim

2 Create/map working library

GUI File→Change Directory→ *{path to design directory}*
Library→Create a New Library→A new library and a logical mapping to it→ *{work}* *{relative path to work}*

Command **cd** *{path to design directory}*
vlib *work*
vmap *work ./work*

3 Map to technology libraries

GUI Library→Create a New Library→a map to an existing library: *{Unisim* **or** *xc4000xl** **or** *Simprim}*
*Verilog Unisim: Use specific technology name
{path to library}

Command **vmap** *{library name}*
{path to compiled library}

4 Compile input files

GUI Compile→Library: *{work}* Filename: *{name of file}*
→Compile→Done

Command **vcom -work** *work {file}*
vlog -work *work {file}*

5 Simulate

GUI VSIM→Design
Simulator Resolution: *ns* Library: *work* Simulate: *{select testbench}*
File→Load Design→Library: *{Select library name}*
Simulate: *{Select testbench}*
SDF: *{Select SDF dile}*→Add Load
View→all
Signals→ *{Select signals}*→View wave→ Selected signals
Run

Command **vsim -t** *ns* **-lib*** *work* **-sdftyp** */UUT** **=** *{SDF file} {testbench}*
*-L for Verilog
*Substitute top-level design instance name within testbench
VSIM→run *{length of testbench in ns}*