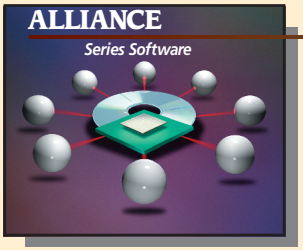

XILINX®

Mentor•Xilinx Design Flow

Module Generators

To ModelSim Simulator

.V .VHD

LogiBLOX

CORE Generator

Must be invoked inside of PLD-DA to create symbol

CORE Generator and LogiBLOX can be invoked as stand-alone for HDL outputs.

Design Architect pld_da

EDN

To QuickSim

.VEI .VHI

VEO VHO

EDDM

pld_dmgr

pld_men2edif

HDL Editor

Renoir

pld_dve

pld_edif2tim

EDIF

NGC

.NGC= Xilinx Binary Netlist

HDL

To ModelSim Simulator

Design Viewpoint

EDDM

CORE Generator

LogiBLOX

UNIFIED Gates

UniISim

SimPrim

HDL Test Bench

Command File or Test Vectors

QuickSim

QuickSim Pro

ModelSim

SIMULATOR

EDIF

VHDL Verilog

SDF

Timing Simulation Flow

BIT JEDEC

Reports

.MOD .DATA

TAV Board Level Timing Analysis

Xilinx

IMPLEMENTATION

Tools

Timing Requirements

LEONARDO SPECTRUM

EDIF

NCF

VHDL Verilog

To ModelSim Simulator

User Constraints File

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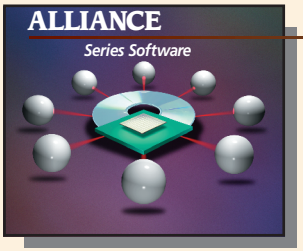

Xilinx•Mentor Design Guide

Device Architecture Support

FPGA Product Family
- Spartan
- Virtex
- XC4000X

CPLD Product Family
- XC9500

Xilinx Contacts and Technical Support

World Wide Web:
http://www.xilinx.com

North America
1-800-255-7778
hotline@xilinx.com
United Kingdom
44 1932-820821
ukhelp@xilinx.com

France
33 1-3463-0100
frhelp@xilinx.com
Japan
81 3-3297-9163
jhotline@xilinx.com

Mentor Contacts and Technical Support

World Wide Web:
http://www.mentorg.com
North America
1-800-547-3000
support@mentorg.com

Recommended Settings

```
Setenv MGC_HOME path_to_mentor_software
Setenv XILINX path_to_Xilinx_software
Setenv LCA $Xilinx/mentor/data
Setenv SIMPRIMS $XILINX/mentor/data/
simprims
set path=(${XILINX}/bin/platform(sol or hp)\
        ${XILINX}/mentor/bin/platform\
```

Solaris (additional)

```
setenv LD_LIBRARY_PATH
/user/openwin/lib:$MGC_HOME/shared/
lib:$MGC_HOME/lib:/usr/lib:${XILINX}/bin/sol
setenv LD_BREADTH 1
```

Recommended Settings Continued

HP (additional)

```
setenv SHLIB_PATH
$MGC_HOME/shared/lib:$MGC_HOME/lib/usr/
lib:${XILINX}/bin/hp
```

Guide Overview

1 Invoke the Design Manager

pld_dmgr

2 Schematic Design Flow

- Use Design Architect (**pld_da**) to create schematic design.
- Run **pld_dve** and generate a Design Viewpoint.
- Use **pld_quicksim** to conduct Functional Simulation.
- Run **pld_men2edif** and generate EDIF netlist.
- Run **Xilinx Implementation Tools**, perform place, and route and generate timing EDIF file.
- Run **pld_edif2tim** on timing EDN file and perform timing simulation using **pld_quicksim**.

3 HDL Design Flow

- Enter the HDL Design in **Renoir, Text Editor** or **HDL Editor**.
- Conduct Functional Simulation using **QuickSim Pro** (mixed schematic) or **ModelSim**.
- Run **Leonardo Spectrum** or 3rd party synthesis tool and generate EDIF netlist.
- Run **Xilinx Implementation Tools**, perform place and route and generate post-routed VHDL/Verilog and SDF Timing files.
- Conduct Timing Simulation using **ModelSim**.

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