IMA-32 Inverse Multiplexer for ATM

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Features

- Fully Compliant with the ATM Forum Inverse Multiplexer for ATM (IMA) specification
- Supports the 8/16 bit UTOPIA Level 2 specification
- IMA Programmable Features
  - Number of Groups, 1-16
  - Number of Links, 1 - 32
  - Assignment of facilities to groups or pass-through
  - Differential Delay Compensation
  - IMA Frame Size (32, 64, 128, 256)
  - Transmit Clock Mode
  - Symmetrical / Asymmetrical Configuration and Operation
- IMA Date Cell Rate (IDCR) implementation
- IMA Device Driver software available
  - Simplifies Configuration and Status Reporting
  - Supports IMA MIB
  - Provides group start-up procedures
  - Controls link addition/deletion procedures
  - IMA Layer Failure Monitoring
  - IMA Layer Performance Monitoring
- Includes Diagnostics for external memory devices
- Chip solution provided for the specific IMA implementation

AllianceCORE™ Facts

Core Specifics		
Supported Family	**XC4000XLA**	**Virtex-E**
Device Tested	XC4085XLA-09BG352C	XCV600E-6BG432C
CLBs/CLB Slices	3136	TBD[1]
Clock IOBs	3	3
IOBs	258	214
Performance (MHz)	50	50
Xilinx Tools	M1.5i or later	M2.1i or later
Special Features	SelectRAM	SelectRAM, BlockRAM
Provided with Core		
Documentation	Product Brief Specification/Design Document Product Summary Software Specification	
Design File Formats	ViewLogic Schematic source or PROM files	VHDL source or PROM files
Constraints File	UCF file	
Verification	Through ModelSIM and hardware evaluation board	
Instantiation Templates	None	
Reference designs & application notes	EP-IMA Hardware Evaluation Platform Schematic Reference Design	
Additional Items	DRV-IMA Software Device Driver	
Simulation Tool Used		
Modelsim PE V5.2e		
Support		
Support provided by Applied Telecom Inc.		

Note:
1. Contact Applied Telecom for latest CLB Slice count.

Applications

- Network access equipment such as adapters, multiplexers, routers, and switches
- Public/private UNI, NNI, and B-ICI applications

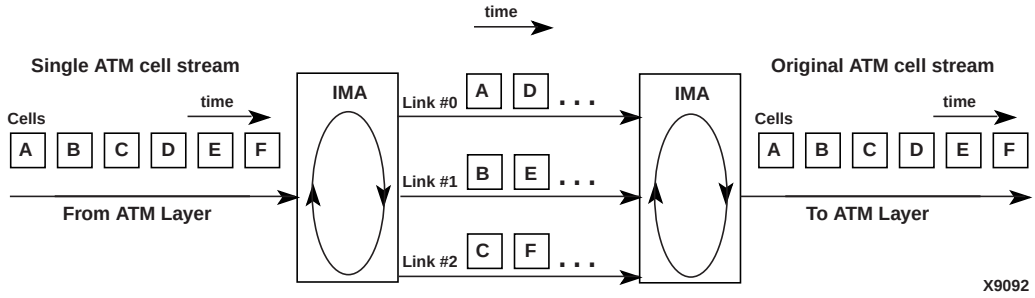


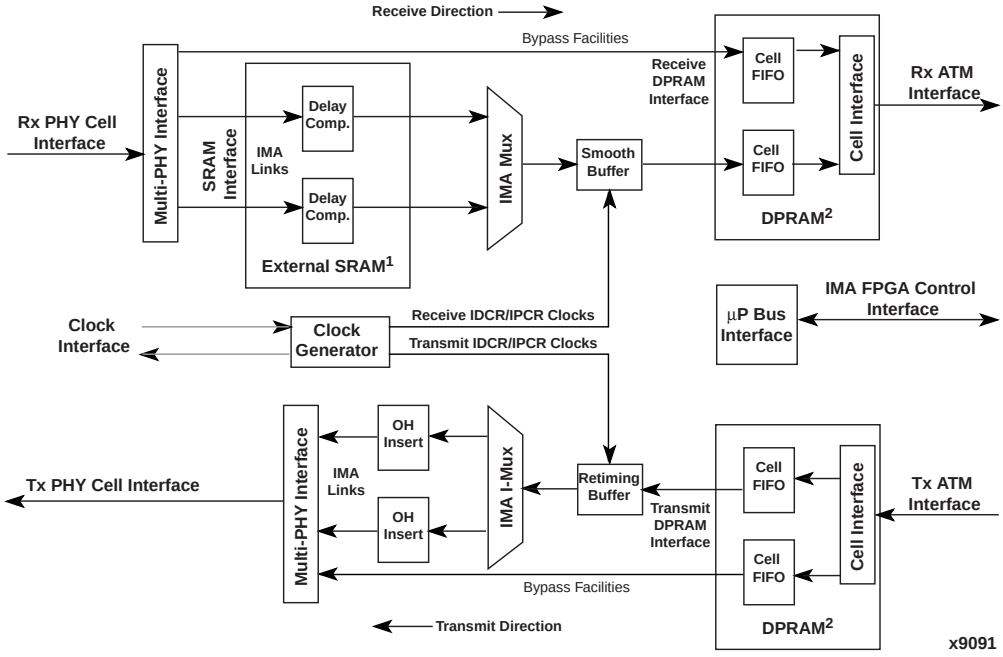
Figure 1: Simplified IMA Diagram

General Description

The IMA products implement the ATM Forum Inverse Multiplexing for ATM (IMA) specification. The IMA specification uses a cell based multiplexing technique for converting a single ATM stream into multiple lower speed ATM streams for transmission over independent links. Applied Telecom's IMA32 solution supports 32 physical links and 16 IMA groups with a maximum of 8 physical links per group. Mechanisms are specified for accommodating differential delay variations present in the transmission links and for handling link failures and changes to the available transmission bandwidth. Figure 1 illustrates the basic IMA mechanism for sending a single ATM cell stream over a number of lower speed transmission links.

Functional Description

The Functional Block diagrams shown in Figure 2 and 3 provides an overview of the IMA implementation. It is composed of four main functional areas: the IMA clock generators, the Transmit IMA processing, the Receive IMA processing, and the Microprocessor Bus Interface.



1. XC4085XLA uses asynchronous SRAM, XCV600E requires synchronous RAM
2. XC4085XLA requires external DPRAM, XCV600E uses internal Virtex-E BlockRAM

Figure 2: Functional Block Diagram - Detailed

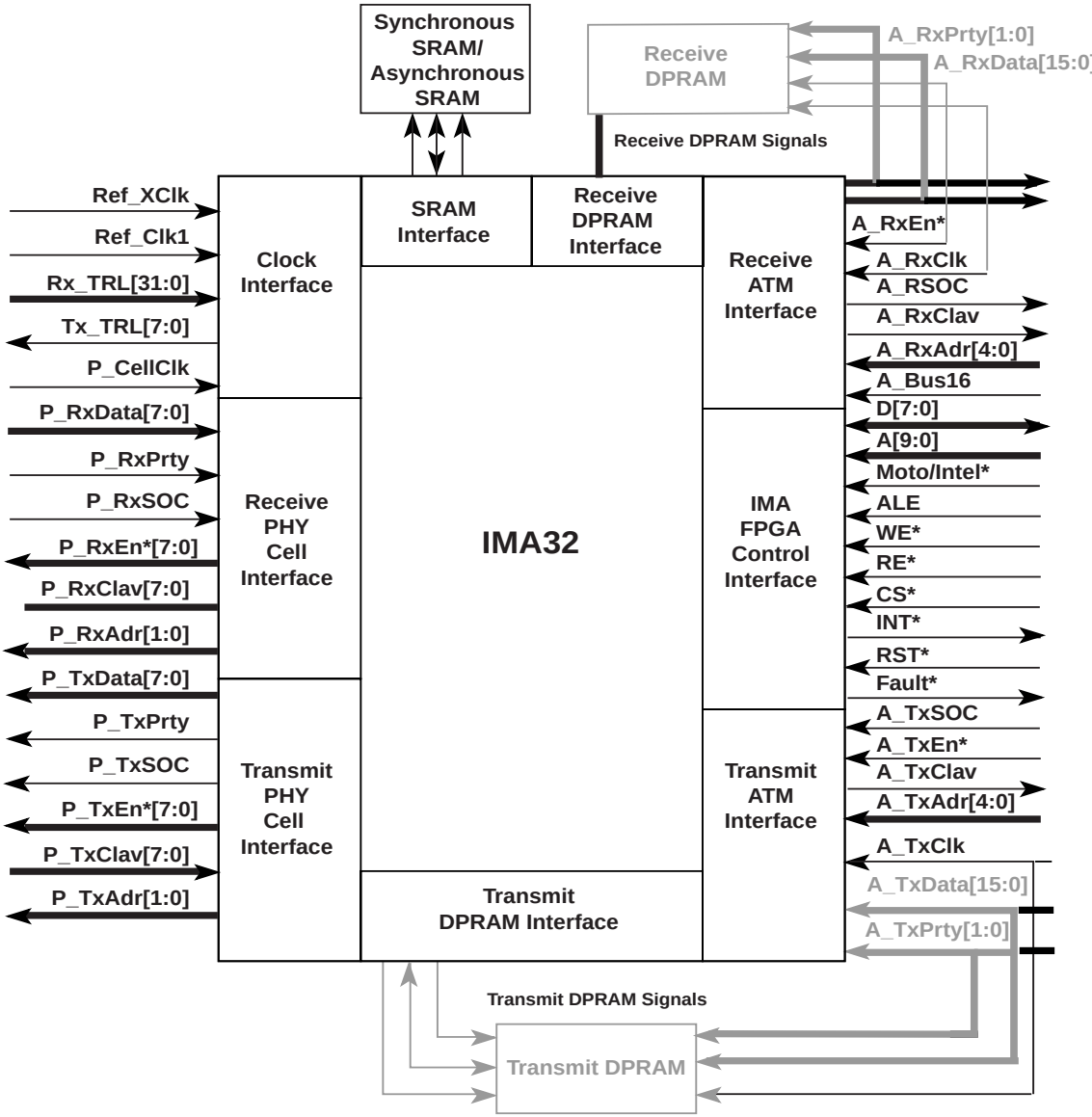


Figure 3: Functional Block Diagram - Overview

IMA Clock Generators

The IMA clock generator is responsible for producing the IMA Data Cell Rate (IDCR) and IMA PHY Cell Rate (IPCR) clocks that are used by both the Receive and Transmit IMA Processors. This block allows for significant flexibility in clocking for both the Transmit and Receive IMA Processors.

Transmit IMA Processing

The Transmit IMA Processing section receives ATM cells from the ATM layer via the Utopia Transmit ATM Interface (Tx ATM I/F). In the Xilinx 4000 series implementation, this interface connects to external DPRAMs. In the Xilinx Virtex E implementation, the external DPRAMs are absorbed into the FPGA using the BlockRAM, and the ATM cell interface connects directly to the Virtex E device. The Retiming Buffer extracts the received transmit ATM cells to synchro-

nize the data according to the Transmit IMA Data Cell Rate (Transmit IDCR) clock. The IMA I-Mux inverse multiplexes the Transmit ATM Interface data into the individual IMA links. The OH Insert block generates the IMA frame and inserts the ICP, SICP, and Filler cells for each IMA link. The IMA encoded cell stream is then passed to the Transmit PHY Cell Interface (Tx PHY Cell I/F). The Transmit PHY Cell Interface serves as a Utopia Level 2 master to one or multiple PHY devices. These PHY devices encapsulate the ATM cell data for transmission over the T1/E1 facility link. The Transmit IMA Processor also provides Bypass Facilities to allow individual T1/E1 links to operate in a pass-through mode allowing ATM cell data to be passed from the Transmit ATM Interface to the Transmit PHY Cell Interface without IMA processing.

Receive IMA Processing

The Receive IMA Processing section provides the inverse operation of the Transmit IMA Processor. The Receive IMA Processor accepts cell streams from multiple T1/E1 links via the Utopia Level 2 Receive PHY Cell Interface (Rx PHY Cell I/F). The Receive PHY Cell Interface data is monitored for IMA framing, and then written to the external SRAM memory via the SRAM I/F. The SRAM memory provides storage for Delay Compensation, which is necessary because of the variable delay paths which occur when receiving ATM cell data over multiple T1/E1 links. The IMA Mux extracts the realigned cell data from the SRAM I/F and removes the IMA control overhead. The cell data is then multiplexed into higher speed ATM cell streams according to the assigned IMA groups. The Smooth Buffer is used to retime the cell data according to the Receive IMA Data Cell Rate (Receive IDCR) clock and then passed to the DPRAM which provides a cell FIFO for the Receive ATM Interface (Rx ATM I/F). The Receive ATM Interface distributes the cells to the ATM layer. The Receive IMA Processor also provides Bypass Facilities to allow individual T1/E1 links to operate in a pass-through mode allowing ATM cell data to be pass from the Receive PHY Cell Interface to the Receive ATM Interface without IMA processing.

Microprocessor Bus Interface

The IMA FPGA Control Interface provides a standard Motorola or Intel compatible microprocessor bus interface for configuration, control, and status. The DRV-IMA software available from Applied Telecom, uses this interface to communicate with the IMA core.

Core Modifications

Since the IMA cores are targeted towards specific Xilinx devices and typically utilize the entire targeted device, it is not recommended that the customer include any significant additional functions in the same device with an IMA core. Please contact Applied Telecom for further information or to discuss additions to the IMA core designs.

Pinout

Applied Telecom's IMA solutions utilize the entire FPGA device and are offered as complete chip solutions for specific device packages. Signal names are shown in the block diagram in Figure 3 and described in Table 1.The IMA32 pinout diagram in Figure 3 shows that an external asychronous SRAM and dual-port RAMs are required for the Xilinx 4000 FPGA implementation while the Virtex-E implementation uses a single external ZBT SRAM and internal dual-port RAMs.

Verification Methods

The IMA core designs were verified through extensive lab and inter-vendor interoperability testing. The IMA core designs have been incorporated by more than 10 companies and have been tested successfully with IMA network equipment products offered by more than 10 additional companies.

Core Assumptions

The IMA32 core fully complies with the ATM forum Inverse Multiplexing for ATM specification versions 1.0 and 1.1.

Recommended Design Experience

Knowledge of ATM technology and ATM Forum specifications is needed.

Available Support Products

Applied Telecom offers the DRV-IMA software program that configures and controls the IMA FPGA core devices to complete the standards compliant IMA implementation. Additionally, an IMA evaluation/test system is available that combines the IMA FPGA based solution with the DRV-IMA software and multiple T1 or E1 facility interfaces.

Ordering Information

For information on this or other products mentioned in this specification, contact Applied Telecom directly using the information provided on the first page.

Related Information

The ATM Forum

The ATM Forum publishes specifications regarding ATM. For more information, contact them as follows:

ATM Forum
Worldwide Headquarters
2570 W. El Camino Real, Suite 304
Mountain View, CA 94040-1313
Tel: +1 650-949-6700
Fax: +1 650-949-6705
E-mail: info@atmforum.com
URL: www.atmforum.com

Xilinx Programmable Logic

For information on Xilinx programmable logic or development system software, contact your local Xilinx sales office, or:

Xilinx, Inc.
2100 Logic Drive
San Jose, CA 95124
Phone: +1 408-559-7778
Fax: +1 408-559-7114
URL: www.xilinx.com

For general Xilinx literature, contact:

Phone: +1 800-231-3386 (inside the US)
+1 408-879-5017 (outside the US)
E-mail: literature@xilinx.com

For AllianceCORE™ specific information, contact:

Phone: +1 408-879-5381
E-mail: alliancecore@xilinx.com
URL: www.xilinx.com/products/logicore/alliance/tblpart.htm

Table 1: Core Signal Pinout

Signal	Signal Direction	Description
Clock Interface		
Ref_XClk	Input	IMA Subsystem clock. Most of the IMA logic circuits use this clock (or a derivative of it). It can also be used as a T1/E1 clock. • o For E1 facilities, use 49.152 MHz (24 * 2.048 MHz) ± 50 ppm • o For T1 facilities, use 37.056 MHz (24 * 1.544 MHz) ± 32 ppm
P_CellClk	Output	Clock signal used for the transfer of Receive and Transmit PHY cells between the PHY device and the IMA FPGA.
Rx_TRL[31:0]	Input	Receive Reference Clocks for facility n (where n = 0 to 31). Used for IMA Data Cell Clock generation.
OTx_TRL[7:0]	Output	Transmit Reference Clocks used for the generation of the facility transmit line clock.
Receive and Transmit PHY Cell Interface		
P_RxData[7:0]	Input	Receives 8 bit PHY Cell Data. All received cells are passed to the IMA FPGA.
P_RxPrty	Input	Parity status signal. A parity calculation is performed over P_RxData[7:0] for each clock cycle of P_RxClk. Odd parity is used.
P_RxSOC	Input	Start of Cell synchronization signal for Receive PHY cells. Indicates first byte of the cell placed on the P_RxData[7:0] bus.
P_RxAdr[1:0]	Output	Receive PHY Cell Bus address. Used to identify 1 T1/E1 link in the PHY device. Both address bits may not be used, depending on software configuration.
P_RxEn*[7:0]	Output	Data transfer and output enable for Receive PHY cells. To support different PHY devices, separate enable signals are provided.
P_RxClav[7:0]	Input	Cell Available signals for Receive PHY cells. P_RxClav[n] is active when one or more complete cells can be transferred from the PHY to the IMA FPGA. To support different PHY devices, separate cell available signals are provided
P_TxData[7:0]	Output	8 bit PHY Cell Data to be sent out the PHY facility. The PHY will append the facility overhead prior to generating the output T1/E1 signal.
P_TxPrty	Output	Parity status signal. A parity calculation is performed over P_TxData[7:0] for each clock cycle of P_TxClk. Odd parity is used.
P_TxSOC	Output	Start of Cell synchronization signal for Transmit PHY cells (active high). Indicates that the first byte of a cell is being placed on the P_TxData[7:0] bus.
P_TxAdr[1:0]	Output	Transmit PHY Cell Bus address. Used to identify 1 T1/E1 link in the PHY device. Both address bits may not be used, depending on software configuration.
P_TxEn*[7:0]	Output	Data transfer enable for Transmit PHY cells. To support different PHY devices, separate enable signals are provided
P_TxClav[7:0]	Input	Cell Available signals for Transmit ATM cells. When P_TxClav[n] is active high, the PHY has space available for one or more complete cells. To support different PHY devices, separate cell available signals are provided.

Table 1: Core Signal Pinout (Cont.)

Signal	Signal Direction	Description
Receive and Transmit ATM Interface		
A_Bus16	Input	Signal which selects the width of the ATM bus for IMA32. When the signal is high, 16 bit UTOPIA operation is enabled. Set this signal low for 8 bit UTOPIA operation.
A_RxClk	Input	Clock signal used for transfer of Receive ATM cells to the ATM Layer. The maximum clock rate is 33 MHz for IMA32 and its derivatives.
A_RxEn*	Input	Data transfer and output enable for Receive ATM cells. This signal enables transfer of A_RxData[7:0] and turns on A_RxSOC and A_RxPrty[0] outputs.
A_RxSOC	Tristated output	Start of Cell synchronization signal for Receive ATM cells. Indicates that the first byte/word of the 53 byte cell is being placed on the A_RxData[7:0] bus.
A_RxAdr[4:0]	Input	Receive ATM Cell Bus address determines the source channel of the Receive ATM cells output from the IMA subsystem and also selects the channel sourcing the A_RxClav signal.
A_RxClav	Tristated output	Cell Available signal for Receive ATM cells. When A_RxClav is active, one or more complete cells can be transferred to the ATM Layer.
A_RxData[15:0]	Tristated output	Receive direction ATM side cell data.
A_RxPrty[0]	Tristated output	Parity status signal. In 8 bit Utopia mode, a parity calculation is performed over A_RxData[7:0] for each clock cycle over A_RxClk. Odd parity is used. In 16 bit Utopia mode, this signal may either be the parity of A_RxData[7:0] or A_RxData[15:0], depending on the configuration of a microprocessor register.
A_RxPrty[1]	Tristated output	Parity status signal used in 16 bit Utopia mode. A parity calculation is performed over A_RxData[15:8] for each clock cycle of A_RxClk. Odd parity is used.
A_TxClk	Input	Clock signal used for transfer of Transmit ATM cells from the ATM Layer. The maximum clock rate is 25 MHz for 8 bit UTOPIA operation and 33 MHz for 16 bit UTOPIA operation.
A_TxEn*	Input	Data transfer enable for Transmit ATM cells (active low). Indicates that the first byte/word of the 53 byte cell is being placed on the A_TxData[ ] bus.
A_TxSOC	Input	Start of Cell synchronization signal for Transmit ATM cells (active high). Indicates that the first byte/word of the 53 byte cell is being placed on the A_TxData[ ] bus.
A_TxAdr[4:0]	Input	Transmit ATM Cell Bus address. This address determines the destination channel of the Transmit ATM cells input to the IMA subsystem and also selects the channel sourcing the A_TxClav signal.
A_TxClav[3:0]	Tristated output	Cell Available signals for Transmit ATM cells. Each signal indicates the cell available status for 8 ATM addresses (listed below).
A_TxData[15:0]	Input	Transmit direction ATM side cell data.
A_TxPrty[0]	Input	Parity status signal. In 8 bit Utopia mode, a parity calculation is performed over A_TxData[7:0] for each clock cycle of A_TxClk. Odd parity is used. In 16 bit Utopia mode, this signal may either be the parity over A_TxData[7:0] or A_TxData[15:0], depending on the configuration of a microprocessor register.
A_TxPrty[1]	Input	Parity status signal used in 16 bit Utopia mode. A parity calculation is performed over A_TxData[15:8] for each clock cycle of A_TxClk. Odd parity is used.
Control Interface		
D[7:0]	Input/Output	Data Bus; 8 bit microprocessor interface.
A[9:0]	Input	Microprocessor interface Address Bus. Both multiplexed and non-multiplexed address /data bus applications supported.

Table 1: Core Signal Pinout (Cont.)

Signal	Signal Direction	Description
Moto/Intel*	Input	Control signal determining the operation of the IMA Control Interface. If set high, the IMA FPGA is compatible with typical Motorola microprocessors. If set low, the IMA FPGA is compatible with typical Intel microprocessors. This signal affects the behavior of the RE*, WE*, and CS* signals.
ALE	Input	Address Latch Enable. This signal is typically used for multiplexed address/ data bus applications.
RE*	Input	Microprocessor bus read enable. This signal is only driven in Intel mode.This signal is combined with CS* to define the time that a read operation is valid.
WE*	Input	Microprocessor bus write enable. This signal is valid in both Intel and Motorola mode.This signal is combined with CS* to define the time that a write operation is valid
CS*	Input	Microprocessor bus chip select
INT*	Output	Microprocessor bus interrupt request signal
RST*	Input	IMA reset (level sensitive)
Fault*	Input	Status signal indicating that a fault has occurred either due to the FPGA failing to configure or due to some fault internal to the IMA implementation in the FPGA
Receive Asynchronous SRAM Interface - 4000XLA[2] only		
R_Sr_Data[7:0]	Input/Output	Receive SRAM Data Bus. ATM cells extracted from the Receive facilities are written into and out of the SRAM for the purpose of differential delay compensation.
R_Sr_Adr[18:0]	Output	Receive SRAM Address Bus. The SRAM address space has been defined to accommodate up to 4 times the ATM Forum requirement for differential delay compensation (25 ms) of T1/E1 facilities.
R_Sr_We*	Output	Receive SRAM write enable signal.
R_Sr_Ce*[1:0]	Output	Receive SRAM Device Select control signals. R_Sr_Ce*[0] is the main SRAM select signal and is always used. R_Sr_Ce*[1] may be optional.
Receive Synchronous SRAM Interface - Virtex-E[3] only		
R_Sr_Data[15:0]	Input/Output	Receive SRAM Data Bus. ATM cells extracted from the Receive facilities are written into and out of the SRAM for the purpose of differential delay compensation.
R_Sr_Adr[18:0]	Output	Receive SRAM Address Bus. The SRAM address space has been defined to accommodate up to 4 times the ATM Forum requirement for differential delay compensation (25 ms) of T1/E1 facilities.
R_Sr_Clk	Output	Receive SRAM clock signal.
R_Sr_We*	Output	Receive SRAM write enable control signal.
R_Sr_We_L*	Output	Receive SRAM low byte (bits 7:0) write enable control signal.
R_Sr_We_H*	Output	Receive SRAM high byte (bits 15:8) write enable control signal.
R_Sr_Ce*	Output	Receive SRAM Device Select control signal.
R_Sr_Oe*	Output	Receive SRAM Device Output control signal.
Receive Dual-Port RAM Interface - XC4000XLA[2] only		
P_RDP_Data[8:0]	Input/Output	PHY side Receive Dual-port RAM Address Bus. This port of the DPRAM is normally written by the FPGA. For diagnostic purposes, the port can also be read-back. The data bus is synchronous with P_RDP_Clk
P_RDP_Adr[11:0]	Output	PHY side Receive Dual-port RAM Address Bus. The address bus is synchronous with P_RDP_Clk.
P_RDP_We*	Output	PHY side Receive Dual-port RAM write enable signal. This signal is synchronous with P_RDP_Clk.

Table 1: Core Signal Pinout (Cont.)

Signal	Signal Direction	Description
P_RDP_Ce*[1:0]	Output	PHY side Receive Dual-port RAM chip select control signals. These signals are synchronous with P_RDP_Clk.
P_RDP_Clk	Output	PHY side Receive Dual-port RAM clock signal.
A_RDP_Adr[11:0]	Output	ATM side Receive Dual-port RAM Address Bus. The address bus is synchronous with A_RxClk.
A_RDP_We*	Output	ATM side Receive Dual-port RAM write enable signal. This signal is synchronous with A_RxClk.
A_RDP_Oe*	Output	ATM side Receive Dual-port RAM output enable signal. This signal is synchronous with A_RxClk.
Transmit Dual-Port RAM Interface - XC4000XLA[2] only		
P_TDP_Data[8:0]	Input/Output	PHY side Transmit Dual-port RAM Data Bus. This port of the DPRAM is normally read by the FPGA. For diagnostic purposes, the port will also be written and read-back. The data bus is synchronous with P_TDP_Clk.
P_TDP_Adr[11:0]	Output	PHY side Transmit Dual-port RAM Address Bus. The address bus is synchronous with P_TDP_Clk.
P_TDP_We*	Output	PHY side Transmit Dual-port RAM write enable signal. This signal is synchronous with P_TDP_Clk.
P_TDP_Ce*[1:0]	Output	PHY side Transmit Dual-port RAM "chip" select signals. These signals are synchronous with P_TDP_Clk.
P_TDP_Clk	Output	PHY side Transmit Dual-port RAM clock signal.
A_TDP_Adr[11:0]	Output	ATM side Transmit Dual-port RAM Address Bus. The address bus is synchronous with A_TxClk.
A_TDP_We*	Output	ATM side Transmit Dual-port RAM write enable signal. This signal is synchronous with A_TxClk.
A_TDP_Ce*	Output	ATM side Transmit Dual-port RAM "chip" select signal. This signal is synchronous with A_TxClk.

1. Signal names with * indicate active low signals; all other signals are active high
2. This interface is used only for the 4000XLA implementation.
3. This interface is used only for the Virtex-E implementation.