



## Perigee, LLC

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## Features

- Supports 4000X, Spartan, Spartan™-II, Virtex™, and Virtex™-E devices
- Converts digital RGB to digital component (YCrCb) video
- Optimized for specific Xilinx architecture
- High-speed operation for HDTV applications
- One conversion per clock cycle--throughput
- Low latency: 6 clock cycles
- VHDL source code and test bench included with core

AllianceCORE™ Facts	
<b>Core Specifics</b>	
See Table 1	
<b>Provided with Core</b>	
Documentation	Core Design Document
Design File Formats	VHDL source code, EDIF netlist
Constraints File	rgb2yrb.ucf
Verification	Testbench, test vectors
Instantiation Templates	VHDL, Verilog
Reference designs & application notes	None
Additional Items	None
<b>Simulation Tool Used</b>	
Active-HDL 3.5 (Aldec) Modelsim 5.e (Model Technology)	
<b>Support</b>	
Support provided by Perigee, LLC.	

## Applications

Real-time TV Output modulation from digital RGB source

**Table 1: Core Implementation Data**

Supported Family	Device Tested	CLBs	Clock IOBs	IOBs <sup>1</sup>	Performance (MHz)	Xilinx Tools	Special Features
Virtex-E	V100E-8	266 <sup>2</sup>	1	67	202	M2.1i	None
Virtex	V50-6	266 <sup>2</sup>	1	67	165	M2.1i	None
4000E/EX/XL/XLA	4036XL-08	237	1	67	120	M2.1i	None
Spartan/XL	S20-4	237	1	67	77	M2.1i	None

Notes:

1. Assuming all core I/Os are routed off-chip.
2. Utilization numbers for Virtex and Virtex-E are in CLB slices.

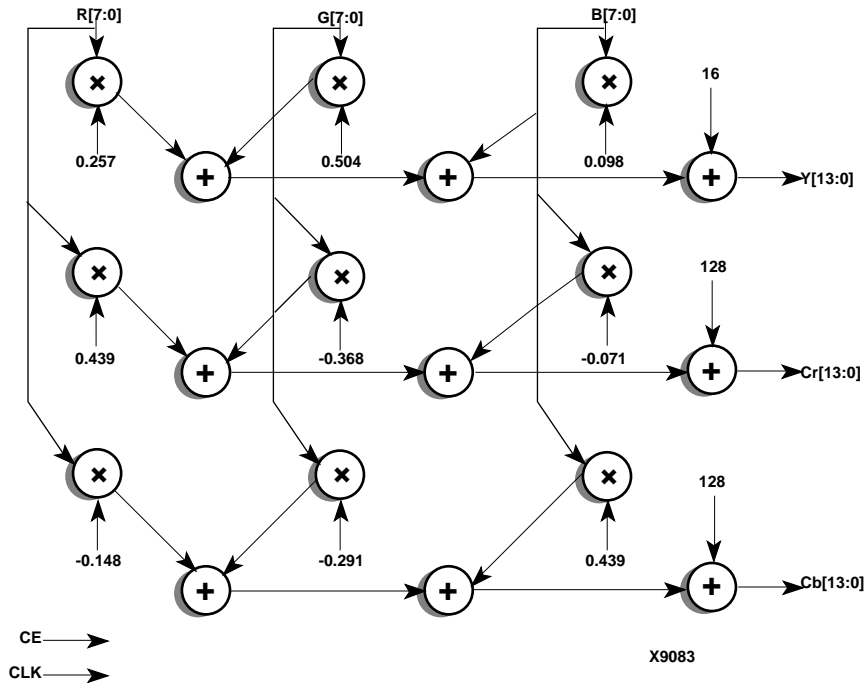


Figure 1: RGB2YCrCb Color Space Converter Block Diagram

## General Description

Most computer graphics systems store video as a set of RGB values for each pixel. To modulate these signals onto a PAL/NTSC video signal, they must be first converted to component video (YCrCb). Figure 1 shows the converter block diagram.

## Functional Description

The RGB to YCrCb color space converter is designed to perform the following equations:

$$\begin{aligned}
 Y &= 0.257 * R + 0.504 * G + 0.098 * B + 16 \\
 Cr &= 0.439 * R - 0.368 * G - 0.071 * B + 128 \\
 Cb &= -0.148 * R - 0.291 * G + 0.439 * B + 128
 \end{aligned}$$

13-bit arithmetic is performed inside this logic core. The full precision of the results are brought out to the outputs of the core. The extra precision can be used or discarded as the user desires.

The core has a latency of 6 clock cycles and a throughput of 1 clock cycle. Both input and output are registered for consistent routing and timing.

## Multipliers

The multipliers are constant-coefficient and are optimized for the Xilinx architecture.

## Core Modifications

The core is available directly from Perigee. Examples of modified versions of this core include:

- RGB2YCrCb with adjusted channel bit widths
- YCrCb2RGB color space converter
- Gamma Correctors

Contact Perigee directly for more information.

## Pinout

The pinout of the color space converter has not been fixed to specific FPGA I/O, allowing flexibility with a user's application. Signal names are shown in Figure 1 and described in Table 2.

## Verification Methods

The core has been tested with a VHDL testbench and test vectors that are provided with the core.

**Table 2: Core Signal Pinout**

Signal	Signal Direction	Description
R[7:0]	Input	Red
G[7:0]	Input	Green
B[7:0]	Input	Blue
CE	Input	Clock Enable
CLK	Input	Clock: Uses one FPGA CLKIOB pin
Y[13:0]	Output	Luminance
Cr[13:0]	Output	Color Red
Cb[13:0]	Output	Color Blue

## Recommended Design Experience

Users should be familiar with video systems and Xilinx development tools.

## Ordering Information

The product as described is available directly from Perigee, LLC.

Perigee also offers services and contract engineering for varying levels of development from logic design to system level embedded and bus-based products. The services include:

- IC design, VHDL or schematic based
- Turnkey hardware/software/firmware development
- System design
- Board design
- DSP and image processing
- Embedded firmware
- GUI and Application software

Perigee's particular area of expertise is in digital video and digital signal processing applications. For more information on Perigee, their products and services, contact them directly.

## Related Information

### Xilinx Programmable Logic

For information on Xilinx programmable logic or development system software, contact your local Xilinx sales office, or:

Xilinx, Inc.  
2100 Logic Drive  
San Jose, CA 95124  
Phone: +1 408-559-7778  
Fax: +1 408-559-7114  
URL: [www.xilinx.com](http://www.xilinx.com)

For general Xilinx literature, contact:

Phone: +1 800-231-3386 (inside the US)  
+1 408-879-5017 (outside the US)  
E-mail: [literature@xilinx.com](mailto:literature@xilinx.com)

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