Xilinx PCI

HotPCI Spartan Prototyping Board

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Introduction

To facilitate rapid development of PCI Designs using the Xilinx LogiCORE PCI32 Interface, VCC has developed the HotPCI Spartan Prototyping Board. This allows the designer to quickly develop, modify, and test Xilinx LogiCORE PCI32 designs in-system. The HotPCI Board is provided with the Xilinx PCI32 Design Kit and should be used in conjunction with the LogiCORE PCI32 Spartan Interface.

Features

The Spartan HotPCI board comes standard with the following hardware and features:

- 5 V PCI 2.1 Compliance
- Xilinx Spartan XCS40-4, reconfigurable via PCI bus or Xchecker cable
- Xilinx XC95108-10 for reconfiguration management
- 8x128K bytes of fast SRAM organized as 2 Independent Banks of 32-bit RAM (four 8-bit x 128K)
- Configuration Flash 128KB for initial configuration
- Configuration RAM Cache 128KB for reconfiguration
- Programmable Clock Generator (360KHz to 100 MHz)
- Mezzanine Connectors for daughter cards
- LEDs to indicate configuration finished (DONE), 5 V, and 3.3 V
- 3 Split Power Planes & 1 Ground Plane
- 4 Signal Layers
- Xchecker/Download Cable Module
- PCI Demo bitstream
- Backend design example files for RAM interface
- PCB design files for the PCI Interface only
- Reference drivers for Windows 95 and Windows NT

Options

All options are available directly from VCC. See the Ordering Information chapter for more details.

- Programmable Voltage Control Module (3.3v to 1.8v)
- License for the Configuration Cache Manager™
- Prototyping Daughter Card
- XC40125 Extended Logic Daughter card
- XC6264 RPU Daughter Card
- HotPCI Card with a Xilinx XC4062XL FPGA

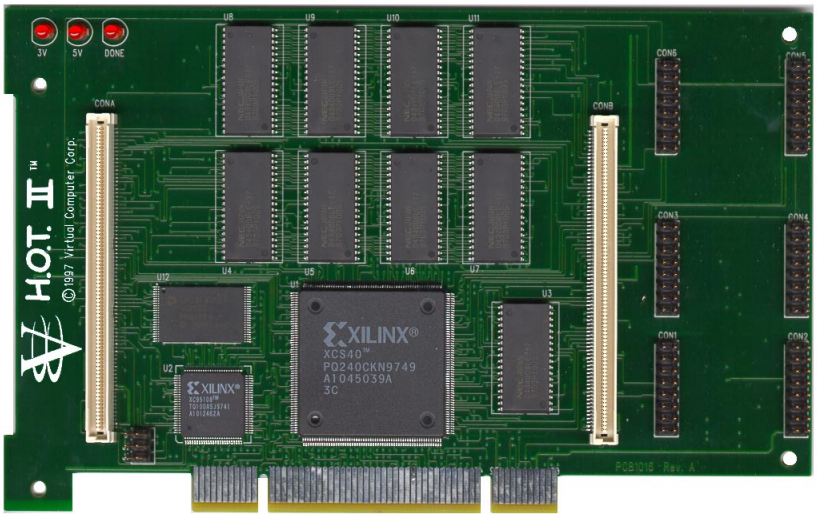

Figure 1: Spartan HotPCI Spartan Prototyping Board

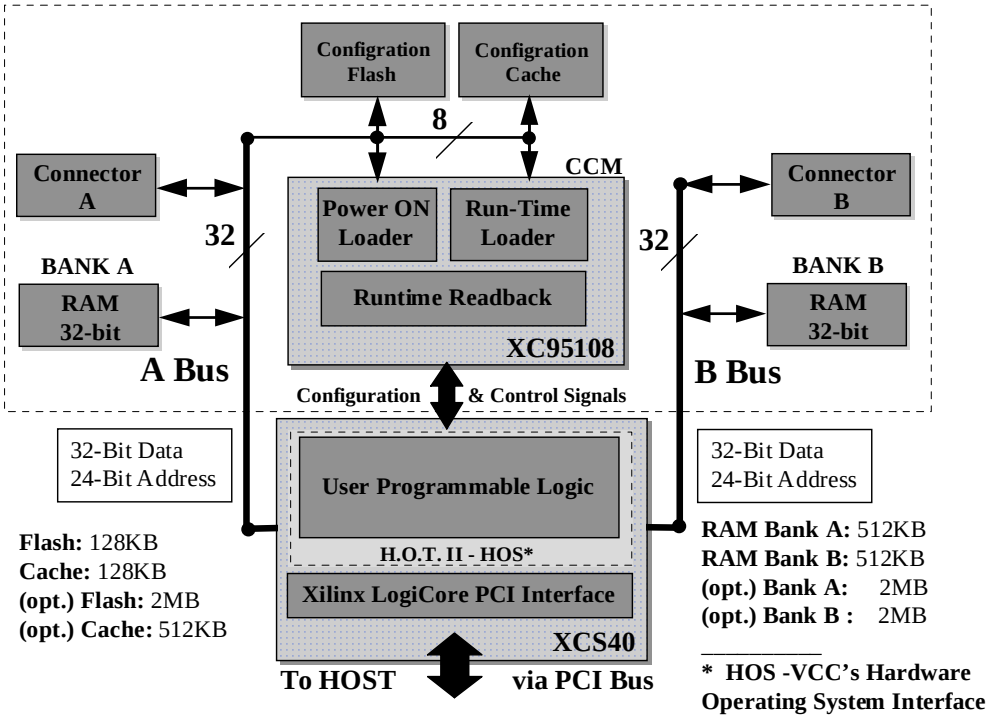

Figure 2: Spartan HotPCI Block Diagram

General Description

The Spartan HotPCI board is a PCI bus based general purpose PCI Prototyping Board, which is provided with the Xilinx PCI32 Design Kit (see the Ordering Information chapter of this data book for details). When used in conjunction with the LogiCORE PCI32 Spartan Interface, designers can quickly modify and test their PCI designs in-system. It features the XCS40 FPGA as the PCI bus interface chip, and a single bank of SRAM plus a VCC proprietary reconfiguration system, the Configuration Cache Manager™ (CCM). The Spartan HotPCI Spartan Prototyping Board is valuable for evaluating, customizing, and verifying the Xilinx LogiCORE PCI32 product line. The mezzanine daughter card connectors offer expandability for prototyping additional features or extending the programmable logic capabilities of the HotPCI board. A series of daughter cards are available from VCC, including a prototyping card for wire-wrap projects, an extended logic card with the XC40125, and a XC6200 Reconfigurable Processing Unit (RPU) card offering microsecond dynamic partial reconfiguration.

Software

The HotPCI Spartan Prototyping Board is supplied with drivers made by Vireo Software, Inc. The Xilinx PCI32 Design Kit also includes driver development tools from Vireo. Together with VCC's HotPCI Board, Vireo's development tools allow easy customization and prototyping of a complete PCI system. See the *Driver::Works Windows Device Driver Development Kit Version 2.0* and the *VtoolsD Windows Device Driver Development Kit Version 3.0* data sheets for more details on the driver development tools. Included with the board is also a bitstream and a Windows '95 application CD that allow demonstration of the card.

Functional Description

The Spartan XCS40 FPGA contains the Xilinx LogiCORE PCI32 Interface Macro and the backend design. VCC supplies a customized backend that allows users to communicate with two fully independent 32-bit banks of RAM and the Configuration Cache Manager™ (CCM). The CCM controls the Run-Time Reconfiguration (RTR) behavior of the system.

The HotPCI board has two independent buses, each with 32-bit data and 24-bit address. There is a daughter board I/O connector for each of these two buses.

Configuration with the CCM

At power-on the FPGA is set to slave serial mode; then the CCM obtains the configuration data from flash and loads the FPGA. Through the PCI bus, the user can load a new

configuration into the Configuration Ram Cache. The user then writes to the CCM to start the reconfiguration of the FPGA. During this time access to the board is disabled by the driver. When the FPGA comes back on-line it signals the driver, which reloads the PCI Header information into the LogiCORE PCI Core. A 128KB Configuration Cache RAM can hold 3 XCS40 configurations. See Figure 2 for a block diagram of the board.

Configuration with an Xchecker cable

Configuration can also be performed through an Xchecker cable or download cable. The supplied Xchecker module occupies one of the daughter card I/O connectors. The PCI bus of the host computer must be reset when this occurs.

Notes: