ADVANCED

Chip Scale & BGA Packaging

New packaging technology for FPGAs and CPLDs reduces board space and increases I/Os.

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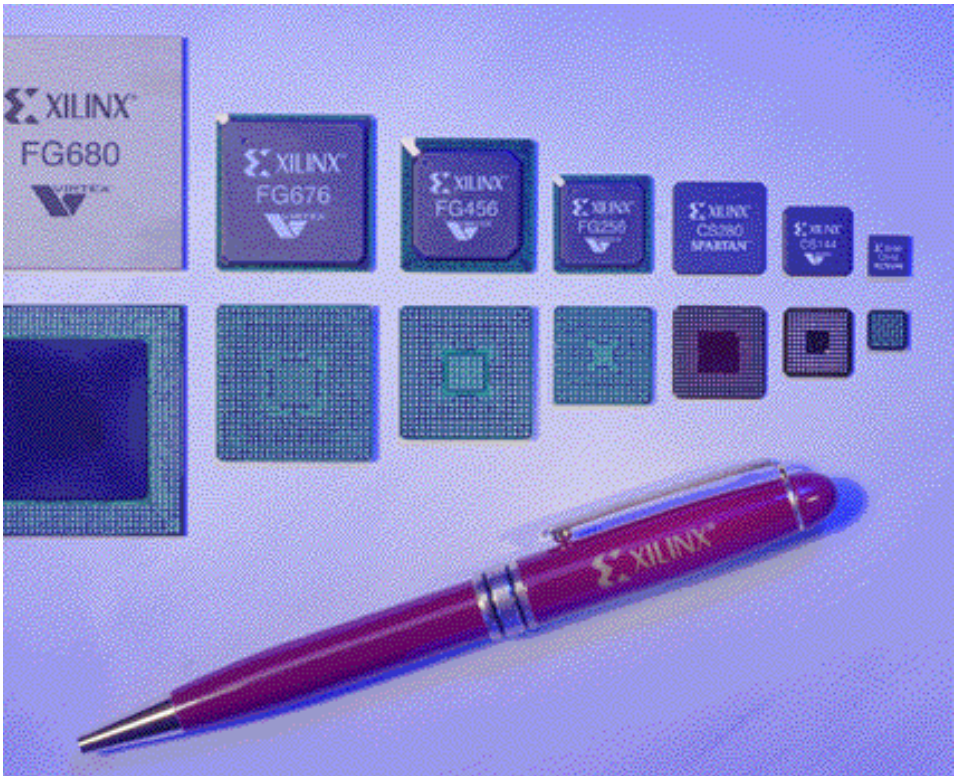
Xilinx recently announced new 144-ball and 280-ball, 0.8-millimeter pitch chip scale packages(CSP) for the SpartanXL FPGA and XC9500 CPLD families. In addition, new 1.0-millimeter FinePitch packages with ball grid arrays ranging from 256 to 680 balls are available for Virtex FPGAs, along with a 144-ball chip scale package for the two smallest Virtex devices.

"Today Xilinx provides more I/Os in less space than any competitor in the industry," said Sandeep Vij, vice president of Marketing and general manager of the High Volume FPGA Business Unit at Xilinx. "We are also the first programmable logic company to be able to offer 100,000 system gates in a compact chip scale package, a remarkable achievement in itself."

New Xilinx Packaging



Chip scale packages are ideal for applications requiring low power and small form factors. The packages are targeted at high-volume, cost-sensitive designs such as digital modems, DVDs, and camcorders. CSP packaging for Xilinx CPLDs and FPGAs offers higher I/O density in less board space than the 1.0 millimeter pitch offerings available from competing programmable logic suppliers.

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Chip Scale Packaging Leadership

Last year, Xilinx was the first programmable logic supplier to offer a 0.8-mm pitch, 48-ball package for the XC9536™ CPLD, providing the smallest form factor package in the industry. This proven chip scale packaging technology is now available for all members of the XC9500 CPLD and SpartanXL FPGA families. The CSP 144–ball package is also available for the Virtex XCV50 and XCV100 devices, which offer 50,000 and 100,000 system gates, respectively. The chip scale packages are designated as the CS48, CS144, and CS280.

Xilinx is the first programmable logic supplier to offer a CSP package that meets the JEDEC Level 3 moisture sensitivity requirements. This level of reliability enables you to reduce standard manufacturing cycle times and further minimize overall system cost.

New Package Lineup

	0.8 mm ChipScale			1.0mm FinePitch			
Leads/balls	CS48	CS144	CS280	FG256	FG456	FG676	FG680
Virtex		x		x	x	x	x
SpartanXL		x	x				
XC9500XV	x	x	x				
XC9500XL	x	x	x				
XC9500	x						

Table 1

FinePitch BGA Packaging for Virtex FPGAs

The new FinePitch ball grid arrays for the Virtex FPGAs are gaining wide market acceptance and feature a 1-millimeter pitch versus the 1.5- and 1.27-millimeter pitch of conventional BGAs. The Virtex series is the first Xilinx FPGA family to fully support these advanced FinePitch BGA packages.

The FinePitch BGAs are available in 256-, 456-, 676-, and 680-ball arrays, require less than half the board space of the previous generation of BGAs, and offer up to 512 user I/Os. Plus, the Virtex series provides footprint compatibility within the FinePitch BGA packages of different density devices. These packages are available for all Virtex devices offering from 100,000 to one million system gates, and are designated as the FG256, FG456, FG676, and FG680.

In addition, Xilinx offers a new dimension of flexibility by supplying vertical pin-out compatibility between the FG456 and FG676 packages. This gives you the ability to layout one printed circuit board and accommodate different solder ball count FinePitch BGA packages, significantly reducing design costs and cycle time.Σ

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