CRC10 Generator and Verifier (CC-130)

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Product Specification

CoreEl MicroSystems

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Features

- Fully compatible with ITU-T Recommendation I.363 for AAL3/4 and ATM OAM Cells
- Single clock operation
- Separate blocks for CRC10 Generator and CRC10 Verifier
- Fully synchronous operation
- Accepts 32 bit data per clock on which CRC10 is computed
- Performance up to 20 MHz giving a throughput of 640 Mbps
- Fully synthesizable Register Transfer Level (RTL) VHDL for FPGA available extra

Applications

The CRC10 Generator and Verifier cores can be used in telecommunications and networking equipment including ATM, SONET and Ethernet systems.

General Description

The CRC10 core is fully compliant to the ITU-T recommendation I.363 for AAL3/4 and ATM OAM Cells. The Core includes both CRC10 Generator and CRC10 Verifier modules. The CRC10 core is fully synchronous with respect to the input clock and is ideally suited to be in a Xilinx FPGA with other high level functions.

Functional Description

The CRC10 Generator and Verifier modules are divided into blocks as shown in Figure 1. Operation of each module is described below.

Note:

AllianceCORE™ Facts

Core Specifics		
Device Family	Spartan	XC4000XL
CLBs - Generator: CLBs - Verifier:	83 46	83 46
IOBs - Generator: IOBs - Verifier:	46[1] 37[1]	46[1] 37[1]
CLKIOBs - Generator: CLKIOBs - Verifier:	1[1] 1[1]	1[1] 1[1]
System Clock f_{max}	20 MHz	20 MHz
Device Features Used	N/A	

Supported Devices/Resources Remaining		
	I/O	**CLBs**
XCS30 PQ208-4 (Gen) XCS30 PQ208-4 (Ver)	83 92	493 530
XC4013XL PQ160-2 (Gen) XC4013XL PQ160-2 (Ver)	83 92	493 530

Provided with Core	
Documentation	Product Brief Specification Document Test Bench Design Document Test Scripts
Design File Formats	VHDL compiled, EDIF netlist
Constraint Files	Generator: crcgen.ucf Verifier: crcver.ucf
Verification Tool	Script Based Behavioral VHDL Test Bench
Schematic Symbols	None
Evaluation Model	Behavioral VHDL
Reference Designs & Application Notes	ITU-T I.363 Specification
Additional Items	None

Design Tool Requirements	
Xilinx Core Tools	Alliance 1.3
Entry/Verification Tool	Model Tech V-System

Support
Support provided by CoreEl Microsystems

1. Assuming all core signals are routed off-chip.

Generator Operation

The CRC10 Generator computes and outputs the CRC10 for a Cell Data. Init Signal sets the CRC10 output to all 0's. The 32 Bit Trace Block computes the 32 bit intermediate

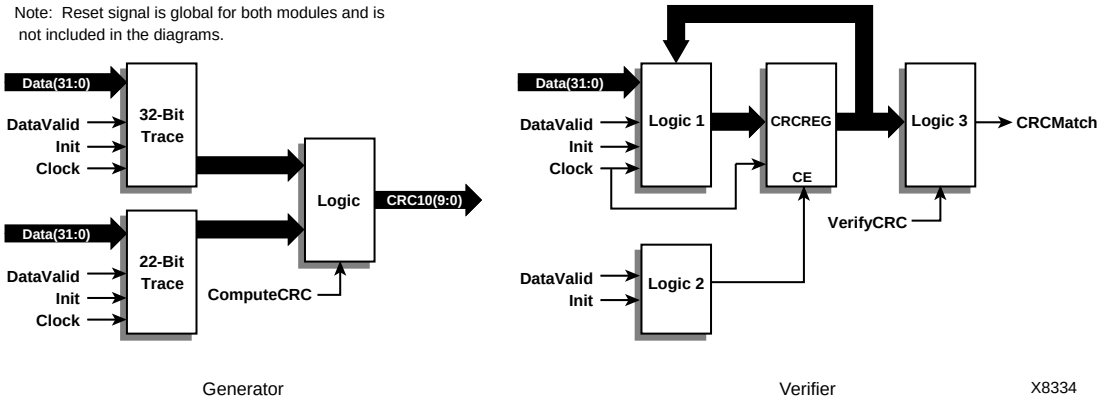

Figure 1: CRC10 Generator and Verifier Block Diagrams

CRC. The 22 Bit Trace Block computes another intermediate 32 bit CRC. The 10 Most Significant Bits of the 32 Bit Trace is selected as the CRC10 remainder when the ComputeCRC is deasserted and the 10 Most Significant Bits of the 22 Bit Trace is selected as the CRC10 remainder when the ComputeCRC is asserted.

Verifier Operation

The CRC10 Verifier computes the CRC10 for the entire cell received and generates a CRCMatch signal if the result is zero. The Init Signal resets the CRCReg Outputs to zero. Once the whole cell is fed, the VerifyCRC signal must be asserted for one clock cycle in order to check the CRCReg Value for zero. If it is zero, the CRCMatch output signal is driven high for one clock cycle.

Core Modifications

Normally, modifications are not possible by the user since the core is provided in a Xilinx netlist format. CoreEI can perform special modifications for additional charge. However source code is available for additional cost where the customer can make modifications. Contact CoreEI Microsystems for more information.

Pinout

The pinout is not fixed to any specific device I/O. Signal names for each module are provided in the block diagrams shown in Figure 1, and described in Table 1.

Verification Methods

This core has been used in larger ASICs and is silicon proven. The FPGA verification was done by back annotating the implementation and simulating in a Model technology V-System environment.

The test bench was written in VHDL with very powerful scripting capabilities and several scripts have been written for verifying the implementation. Additional tests can be added to the testbench by writing new scripts.

Recommended Design Experience

Knowledge of error correction in network systems is needed. User should be familiar with HDL design methodology including FPGA targeting. Using the testbench requires familiarity with V-System of Model Technology.

Available Support Products

CoreEI offers a test bench for verifying the core along with a complete line of ATM Core Cells for Xilinx FPGAs that perform the following functions:

- UTOPIA Interface
- Cell Delineation
- Cell Assembly
- CRC-32

Ordering Information

For information on this or other products mentioned in this specification, contact CoreEI Microsystems directly from the information provided on the front page.

Table 1: Core Signal Pinout.

Signal	Signal Direction	Description
CRC10 Generator Signals		
Data(31:0)	Input	When *DataValid* is asserted, *Data* should be dword of current cell for which CRC10 is computed.
DataValid	Input	Indicates input *Data* is valid and CRC10 to be computed for value on *Data*.
Init	Input	Init Signal sets initial CRC Value to 0; asserted on start of a new cell.
Clock	Input	Used to sample all other inputs; uses FPGA CLKIOB pin.
Reset	Input	Resets outputs to 0; asserted on power-up/reset.
ComputeCRC	Input	When signal is sampled active, CRC10 output gives valid 10 bit CRC to be transmitted with data; asserted along with last dword given to CRC10 Generator.
CRC10(9:0)	Output	Indicates current CRC remainder of cell being processed.
CRC10 Verifier Signals		
Data(31:0)	Input	When *DataValid* is asserted, *Data* should be dword of current cell for which CRC10 is computed.
DataValid	Input	Indicates input *Data* is valid and CRC10 to be computed for value on *Data*.
Init	Input	Init Signal sets initial CRC Value to 0; asserted on start of a new cell.
Clock	Input	Used to sample all other inputs; uses FPGA CLKIOB pin.
Reset	Input	Resets outputs to 0; asserted on power-up/reset.
VerifyCRC	Input	When signal is sampled active, most significant 10 bits of *CRC* output is compared with zero. *VerifyCRC* should be asserted with 32 bit trailer of cell to find if cell was received without errors. *VerifyCRC* is asserted for one clock cycle if cell received is correct.
CRCMatch	Output	Asserted in response to *VerifyCRC* if current CRC remainder matches zero.

Related Information

The ATM Forum

The ATM Forum publishes specifications regarding ATM. For more information, contact them as follows:

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Xilinx Programmable Logic

For information on Xilinx programmable logic or development system software, contact your local Xilinx sales office, or:

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