UTOPIA Slave (CC-141)

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CoreEl MicroSystems

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Features

- Pre-defined implementation for predictable timing in Xilinx FPGA or HardWire[a]
- Conforms to ATM Forums UTOPIA Level 2 specifications, Version 1.0
  - Support for 25 MHz, 33 MHz and 50 MHz operation
- Conforms to cell transfer procedure required in ATM UNI devices
- 8 bit / 16 bit UTOPIA operation
- SPHY operation in both octet-level handshake and cell-level handshake
- MPHY operation in cell level handshake supports up to 31 PHY devices
- Detection and dropping Runt cells on transmit side
- Dropping excess bytes of a cell on transmit side
- Parity verification on transmit side
- Parity indication on receive side
- Optional cell drop on the occurrence of parity error(s) on transmit side
- It supports cell of 52 bytes as well as cell of 53 bytes in case of 8 bit UTOPIA operation and cell of 52 bytes as well as 54 bytes in case of 16 bit UTOPIA operation

AllianceCORE™ Facts

Core Specifics	
Device Family	XC4000XL
CLBs - Transmitter: CLBs - Receiver:	381 - 265
IOBs - Transmitter: IOBs - Receiver:	51[1] 46[1]
CLKIOBs - Transmitter: CLKIOBs - Receiver:	2 2
System Clock f_{max}	50 MHz
Device Features Used	SelectRAM™, Global Clocks

Supported Devices/Resources Remaining		
	I/O[1]	CLBs
XC4020XL-09 BG256 (Tx)	154	403
XC4020XL-09 BG256 (Rx)	159	519

Provided with Core	
Documentation	Product Brief Specification Document Design Document Test Bench Design Document Test Scripts
Design File Formats	VHDL Compiled, XNF netlist
Constraint Files	Transmitter: txut.ucf Receiver: rxut.ucf
Verification Tool	Script Based behavioral VHDL Test Bench
Schematic Symbols	None
Evaluation Model	Behavioral
Reference Designs and Application Notes	UTOPIA Level 2 Specification V1.0.
Additional Items	None

Design Tool Requirements	
Xilinx Core Tools	Alliance 1.3
Entry/Verification Tool	Model Tech V-System

Support
Support provided by CoreEl Microsystems

Note:
1. Assuming all core signals are routed off-chip.

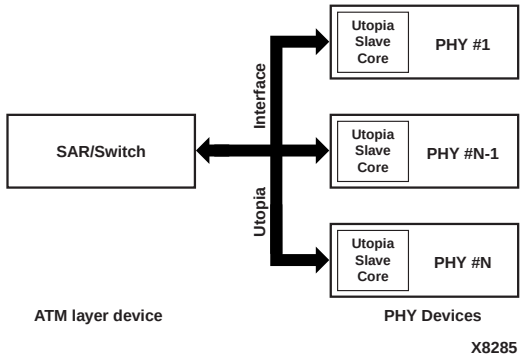

Figure 1: Data transfer between UNI device and a UTOPIA compatible ATM layer device

Applications

The UTOPIA core can be used in Asynchronous Transfer Mode (ATM) networking systems such as adapter cards, routers and switches.

General Description

The Slave UTOPIA Core Cell (SUC) is a UTOPIA Slave that can be used in any Physical Layer Device (PHY) that performs the functions of the Transmission Convergence sublayer. The SUC facilitates data transfer between the UNI (User Network Interface device) and a UTOPIA compatible ATM layer device as shown in Figure 1. In SPHY operation, it supports octet level handshake and cell level handshake. In MPHY operation, it supports up to 31 PHY devices.

Functional Description

The Slave UTOPIA core is architecturally divided into Transmit and Receive blocks as shown in Figure 2 and Figure 3, respectively. Operation of each are described below.

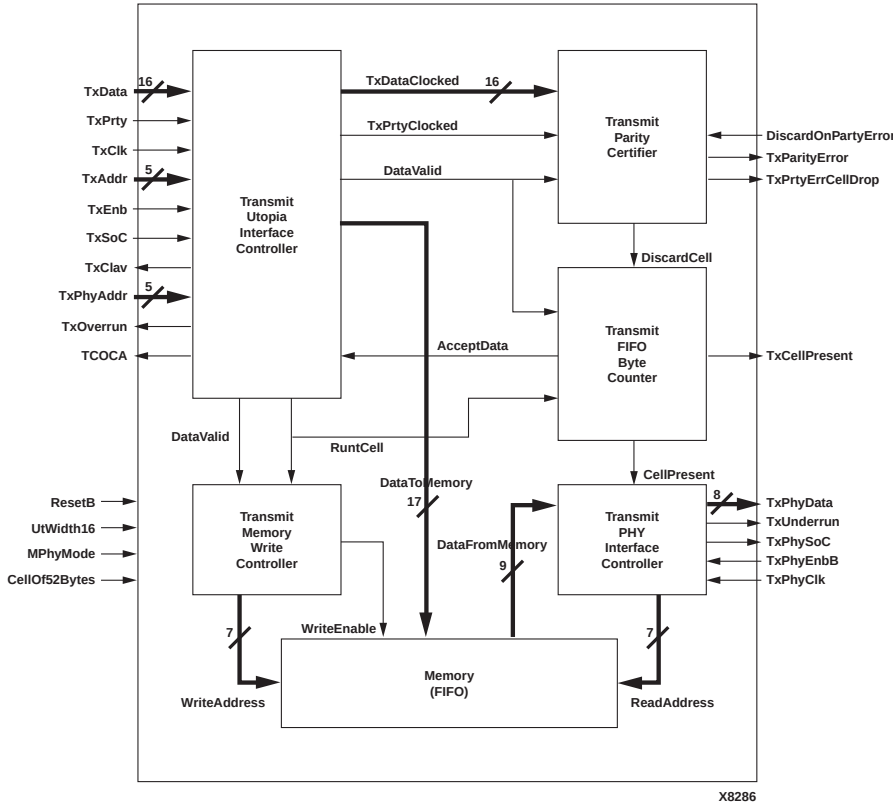

Figure 2:Transmit UTOPIA Block Diagram

Transmitter Block Operation

Transmit UTOPIA provides an industry standard interface between the ATM layer and a PHY device through a 216-Byte (4 cell) deep rate-matching buffer (FIFO). It supports both SPHY and MPHY modes of operation.

The Transmit interface is controlled by the ATM layer. The ATM layer provides an interface clock to the Transmit UTOPIA core for synchronizing all interface transfers. Data flow in the transmit interface is in the same direction as the ATM enable. Signals TxEnb, TxData, TxSoC, and TxPrty are sampled on the rising edge of the TxClk.

It accepts 54, 53, or 52 byte cells from the ATM layer, writes them into an internal FIFO with TxClk. Cells are read from the FIFO with TxPhyClk and sent to a cell processing device (cell processor) within the PHY. It detects and discards runt cells and excess bytes. It also performs parity check and gives the user the option of discarding the cells on the occurrence of parity errors.

The UTOPIA core indicates it can accept data using the TxClav signal, then the ATM layer drives data onto TxData and asserts TxEnb. The UTOPIA core controls the flow of data via the TxClav signal.

Receive Operation

The Receive operation is controlled by the ATM layer. The ATM layer provides an interface clock to the UTOPIA core to synchronize all transfers. The receive interface has data flowing in the opposite direction as the ATM enable.

The ATM receive block generates all output signals on the rising edge of RxClk. Signals RxData, RxSoC, RxPrty and RxEnb are sampled by the UTOPIA core on the rising edge of RxClk.

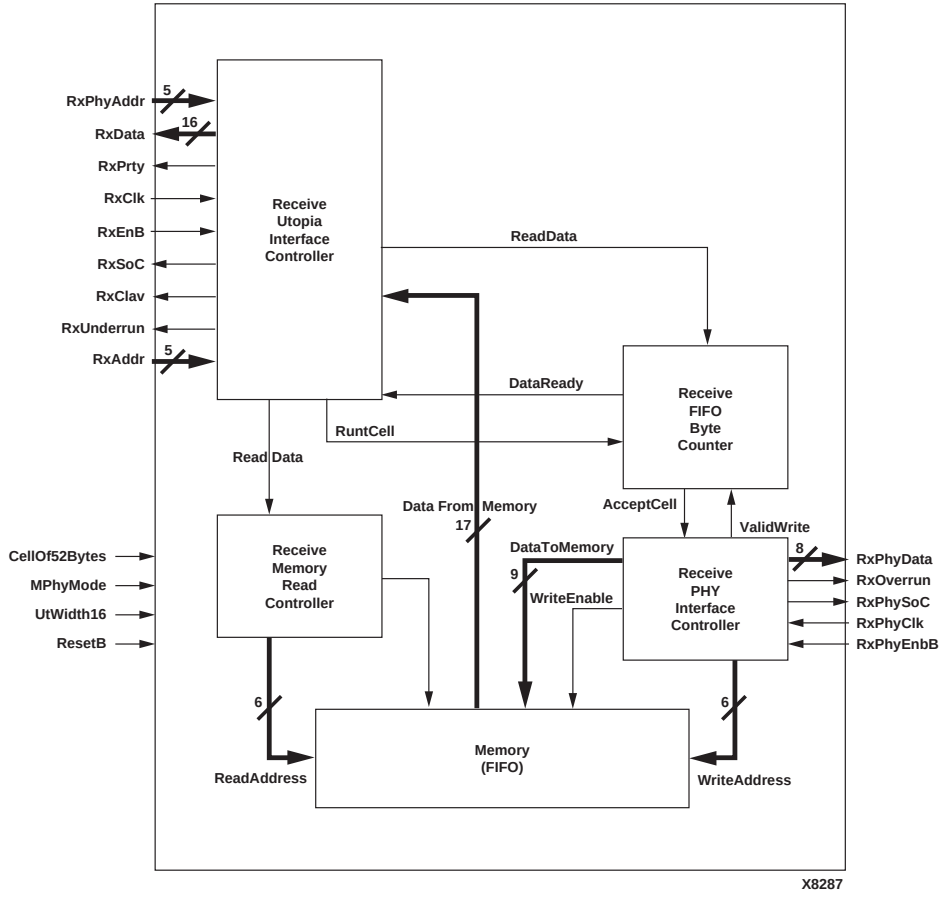

Figure 3: Receive UTOPIA Block Diagram

Receive data is transferred from the UTOPIA core to the ATM layer through the following procedure. The UTOPIA core indicates it has valid data; then the ATM layer asserts RxEnb to read this data from the UTOPIA core. The UTOPIA core indicates valid data via the RxClav signal.

Receive UTOPIA supports both SPHY (Cell-Level handshake or Octet-Level handshake) and MPHY modes of operation. It can accept 53, or 52 byte cells from the cell processing device.

For 16 bit UTOPIA operation, it converts cell of 53 bytes into cell of 54 bytes by adding one junk byte as the 6th byte of the cell, and directly writes them into an internal 108 byte (2 cell) deep rate matching buffer (FIFO) using RxPhyClk. It then reads the cells from the FIFO with RxClk, and sends them to the ATM layer.

It gives 52, 53 or 54 byte cells to the ATM layer depending on Cellof52Bytes and Utwidth16 signals. It generates Odd parity for data on the UTOPIA Interface.

Core Modifications

Normally, modifications are not possible by the user since the core is provided in a Xilinx netlist format. CoreEl can perform special modifications for additional charge. However source code is available for additional cost where the customer can make modifications. Contact CoreEl Microsystems for more information.

Pinout

The pinout is not fixed to any specific device I/O. Signal names for the transmit and receive UTOPIA blocks are provided in the block diagrams shown in Figures 2 and 3, and described in Tables 1 and 2, respectively.

Verification Methods

This core has been used in larger ASICs and is silicon proven. The FPGA verification was done by back annotating the implementation and simulating in a Model technology V-System environment.

The test bench was written in VHDL with very powerful scripting capabilities and several scripts have been written for verifying the implementation. Additional tests can be added to the testbench by writing new scripts.

Recommended Design Experience

Knowledge of ATM technology and UTOPIA Level 2 specifications is needed. User should be familiar with HDL design methodology including FPGA targeting. Using the testbench requires familiarity with V-System of Model Technology.

Table 1: Transmit UTOPIA Block Signal Pinout

Signal	Signal Direction	Description
UTOPIA Transmit Interface		
TxData(7:0)	Input	Least significant octet of transmit data, driven from ATM to PHY. Bit 7 is MSB, bit 0 is LSB in 8-bit data path.
TxData(15:8)	Input	Most significant octet of transmit data, driven from ATM to PHY. Bit 15 is MSB, bit 0 is LSB in 16-bit data path.
TxPrty	Input	Data path parity; odd parity bit over TxData(7:0) in 8 bit mode or over TxData(15:0) in 16 bit mode.
TxClk	Input	Transmit Master Clock; ATM layer provides interface clock to PHY layer to synchronize all information transfers. Uses 1 FPGA CLKIOB pin.
TxAddr[4:0]	Input	Address of MPHY device. True data driven from ATM layer to poll and select appropriate MPHY device (port in presence of multiple TxClav signals); Bit 4 is MSB. Value of address for Tx and Rx UTOPIA of MPHY devices must be identical.
TxEnb	Input	Enable, validates data on TxData lines.
TxSoC	Input	Start of cell indicator.
TxClav	Output	Cell Available; active high signal from SPHY device to ATM layer in SPHY mode; active high tri-state signal from MPHY device to ATM layer in MPHY mode. A polled MPHY device (port) drives TxClav only during each cycle following its address on TxAddr.
TxOverrun	Output	Indicates FIFO full; active high.
TCoca	Output	Indicates change of cell alignment (from either runt cell or a cell with excess bytes).
TxParityError	Output	Indicates parity errors
TxPrtyErrCellDrop	Output	High signal if cell is dropped due to TxPrty error.

Signal	Signal Direction	Description
PHY Layer Transmit Interface		
TxCellPresent	Output	Indication to cell processor of presence of a complete cell in FIFO.
TxPhyData(7:0)	Output	Data output to cell processor; bit 7 is MSB, bit 0 is LSB.
TxUnderrun	Output	Indicates FIFO empty; active high.
TxPhySoC	Output	Start of cell indication to cell processor.
TxPhyEnbB	Input	Read enable; active low. Indicates valid data present on TxPhyData.
TxPhyClk	Input	Cell Clock, from cell processor; synchronizes all information transfers with UTOPIA core. Uses 1 FPGA CLKIOB pin.
Configuration Signals		
TxPhyAddr(4:0)	Input	PHY device address; provided by UNI device.
ResetB	Input	Power-on reset; active low.
UtWidth16	Input	Indicates 16 bit data path; active high.
MPhyMode	Input	MPHY mode indicator; active high.
CellOf52Bytes	Input	Indicates cells of 52 bytes; active high. Low value = cell of 53 bytes when UtWidth16 is low, and = 54 bytes when UtWidth16 is high.
DiscardOnPrty-Error	Input	Indicates cells are discarded on occurrence of parity error; active high

Table 2: Receive UTOPIA Block Signal Pinout

Signal	Signal Direction	Description
UTOPIA Receive Interface		
RxData(7:0)	Output	Low octet of receive data from PHY to ATM; tristated when device (port) not selected by UTOPIA core. Bit 7 is MSB, bit 0 is LSB for 8-bit data path.
RxData(15:8)	Output	High octet of receive data from PHY to ATM; tristated when device (port) not selected by UTOPIA core. Bit 15 is MSB, bit 0 is LSB for 16-bit data path.
RxPrty	Output Tristated	Data path parity; odd parity bit over RxData(7:0) in 8 bit mode or over RxData(15:0) in 16 bit mode. Tristated when device (port) not selected by UTOPIA core.
RxClk	Input	Clock from ATM to PHY; synchronizes all transfers Uses 1 FPGA CLKIOB pin.
RxEnb	Input	Receive Enable; validates data on RxData.
RxSoC	Output Tristated	Start of cell. Tristated for multiple PHYs, and enabled only in cycles following those with RxEnb asserted.
RxClav	Output Tristated	Cell Available. Active high signal from SPHY device to ATM layer in SPHY mode. In MPHY mode, it is active high tri-state signal from MPHY device to ATM layer. Polled MPHY device (port) drives RxClav only during cycle following one with its address on RxAddr lines.
RxUnderrun	Output	FIFO empty indicator; active high.
RxAddr[4:0]	Input	MPHY device address. True data from ATM to MPHY layer to poll and select appropriate MPHY device (port in presence of multiple RxClav signals). Bit 4 is MSB. Value of address for both Tx and Rx UTOPIA of MPHY devices must be identical.

Signal	Signal Direction	Description
PHY Layer Receive Interface		
RxPhyData(7:0)	Input	Data input from cell processor. Bit 7 is MSB, bit 0 is LSB.
RxOverrun	Output	FIFO full indicator; active high.
RxPhySoC	Input	Start of cell indication from cell processor.
RxPhyClk	Input	Cell Clock from cell processor; synchronizes all transfers with UTOPIA core. Uses 1 FPGA CLKIOB pin.
RxPhyEnbB	Input	Indicates valid data on RxPhyData; active low.
Configuration Signals		
RxPhyAddr (4:0)	Input	PHY device address; provided by UNI device.
CellOf52Bytes	Input	Indicates cells of 52 bytes; active high. Low value = cell of 53 bytes when UtWidth16 is low, and = 54 bytes when UtWidth16 is high.
MPhyMode	Input	MPHY mode indicator; active high.
UtWidth16	Input	Indicates 16 bit data path; active high.
ResetB	Input	Power-on reset; active low.
UTOPIA Receive Interface		
RxData(7:0)	Output	Low octet of receive data from PHY to ATM; tristated when device (port) not selected by UTOPIA core. Bit 7 is MSB, bit 0 is LSB for 8-bit data path.
RxData(15:8)	Output	High octet of receive data from PHY to ATM; tristated when device (port) not selected by UTOPIA core. Bit 15 is MSB, bit 0 is LSB for 16-bit data path.
RxPrty	Output Tristated	Data path parity; odd parity bit over RxData(7:0) in 8 bit mode or over RxData(15:0) in 16 bit mode. Tristated when device (port) not selected by UTOPIA core.
RxClk	Input	Clock from ATM to PHY; synchronizes all transfers Uses 1 FPGA CLKIOB pin.

Available Support Products

CoreEl offers a test bench for verifying the SUC along with a complete line of ATM Core Cells for Xilinx FPGAs that perform the following functions:

- Cell Delineation
- Cell Stream Assembly
- CRC-32
- CRC-10

Ordering Information

For information on this or other products mentioned in this datasheet, contact CoreEl Microsystems directly from the information provided on the front page.

Related Information

The ATM Forum

The ATM Forum publishes specifications regarding ATM. For more information, contact them as follows:

ATM Forum
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2570 West El Camino Real, Suite 304
Mountain View, CA 94040-1313
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Xilinx Programmable Logic

For information on Xilinx programmable logic or development system software, contact your local Xilinx sales office, or:

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