Low-Power FPGA Achieves 400 MHz Performance

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This article discusses several techniques for creating low-power designs demonstrated by a 6-digit frequency counter with a maximum frequency input of 400 MHz. When the input frequency is below 10 MHz, current consumption is below 2 mA, and the operating current at 100 MHz input frequency is below 10 mA. This low-power design, which is implemented in an XC4002XL FPGA, has the following characteristics.

- The time base is derived from a 32 kHz oscillator, controlled by a typical watch crystal.
- The 400 MHz input frequency resolution (250 picosecond period) is made possible by pre-scaling the display counter with a binary ripple counter. This means that only one flip-flop in the FPGA must toggle at the incoming frequency. This flip-flop is carefully placed near the input pin and near the clock input. The use of a global clock, which we usually suggest for synchronous designs, is avoided here in order to save power and increase performance.
- The 6-digit BCD counter is synchronous within each digit, but ripples between digits. This takes advantage of the 4-input look-up-table architecture, while also minimizing total power consumption.
- The non-multiplexed LCD display is driven directly from the complementary CMOS outputs. Because the 48 segments and five decimal points each require AC drive voltage without a DC component, the display backplane is driven with a 0 to 3.6-V square wave of 128 Hz, and the individual segments are driven either in phase or out of phase with their backplane. The necessary XOR gating is easily performed in the new XC4000XL output structure; no additional logic is required.
- The control structure is simple and efficient, operating from a 32 kHz oscillator. The basic assumption is that the display must be updated twice a second. A higher or lower update rate would be irritating to the observer. This 500 ms measuring time and 6-digit display means that input frequencies above 100 MHz must be prescaled by a factor 500 before being counted in the BCD counter. Auto-ranging reduces the prescaler for lower frequencies. Below 10 MHz the display has a fixed resolution of 10 Hz, but with leading-zero suppression in the display.

  The whole control structure uses fewer than eight CLBs (12% of the design).
- The low power consumption allows operation on a rechargeable battery. This makes the instrument portable and avoids real problems and certification issues relating to high-voltage line operation.

> *"By paying close attention to the layout and design of your system, you can achieve both high performance and low power consumption, using standard Xilinx FPGAs."*

Conclusion

By paying close attention to the requirements and the structure of your system, you can achieve both high performance and low power consumption, using standard Xilinx FPGAs. ◆