A 200-MHz Pulse Generator

By Peter Alfke

Using XC4000E or XC4000XL devices, you can reliably clock and manipulate data at up to 200 MHz, over the full voltage and temperature range.

In the design example shown in **Figure 1**, the frequency of a commercially available 100-to-200 MHz Voltage Controlled Oscillator (VCO) is divided by any selected power of 2, from 2^0 to 2^{23}, generating an output frequency that covers the range from 12 Hz to 200 MHz.

The output frequency is potentiometer-adjusted over a 2-to-1 range, and is switch-selected over 24 octaves. The frequency scaler uses seven CLBs, and the switch encoder uses six CLBs. Thus, the design, including the switch encoder, uses a total of 13 CLBs — a mere 13% of the smallest XC4000E family device.

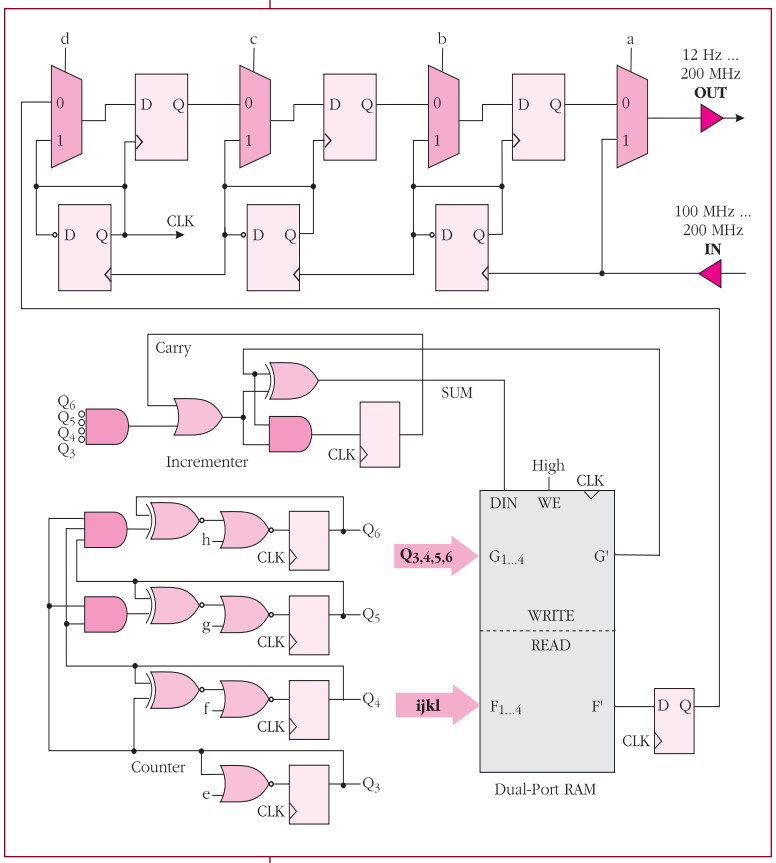

Figure 1 - *A 200 MHz pulse generator with 24 frequency ranges.*

The VCO output clocks one CLB. This CLB is placed directly adjacent to the oscillator input and the output drivers, thus minimizing the speed-critical part of the design. Two additional CLBs complete a 3-bit ripple counter and an output signal multiplexer; because this is an instrument with a single output, there is no reason to design these very fast stages as synchronous counters. However, the remaining 20 binary divider stages are implemented as a synchronous RAM-based state machine, using two CLBs as a counter, one CLB as an adder, and one CLB as a 16-bit dual-port RAM.

Q3 through Q6 address the synchronous RAM, which effectively acts as an adjustable-length shift register. Four control inputs determine the cycle length of the address counters to create a 1-, 2-, 4-, 8-, or 16-bit shift register. The shift register output feeds back to its input through a serial adder, thus implementing a serial incrementer or counter, which is 1, 2, 4, 8, or 16 bits long.

When the read port addresses location zero continuously, it sees a level change for every period of the variable-length address counter. The re-synchronized read output thus divides the RAM clock rate by 2, 4, 8, 16, or 32, as determined by the period of the Q3-Q6 counter.

When the counter divides by 16, the RAM output frequency can be further reduced by advancing the read address. Each address increment reduces the output frequency by a factor of two. A constant read address of all ones creates the lowest output frequency, which equals the RAM clock frequency divided by 2^{20} or the VCO frequency divided by 2^{23}. The 50% duty cycle output frequency can thus be adjusted to any value from 200 MHz to 12 Hz.

This example shows that FPGAs can be used at clock rates that are far above the limitations of conventional synchronous state machine designs. As FPGAs continue to migrate to faster processes, these limits will be pushed even farther, but there will always be an opportunity to achieve the seemingly impossible, through creative understanding of device architecture and I/O capabilities. ◆