Designing With XC9500XL CPLDs

XAPP112 January 22, 1999 (Version 1.1) Application Note

Summary

This application note will help designers get the best results from XC9500XL CPLDs. Included are practical details on such topics as pin migration, timing, mixed voltage interfacing, power management, PCB layout, high speed considerations and JTAG best practices.

Xilinx Family

XC9500XL

Introduction

To get the best performance from any CPLD the designer must be aware of its internal architecture and how the various device features work together. This application note provides useful examples and practical details for creating successful designs. These design techniques apply to all XC9500XL devices because the architecture is uniform across the family.

XC9500XL Architecture

The XC9500XL architecture (Figure 1) bears a strong resemblance to its predecessor, the popular XC9500 family. In the XC9500XL family, a few changes were introduced where significant system improvement could be gained. The resulting family is one which can operate in a standalone 3.3V environment or in mixed 3.3/5V systems or in mixed 3.3/2.5V systems. Propagation delays are as fast as 4 nanoseconds with clock speeds up to 200 MHz. As with the XC9500 family, the XC9500XL family part numbering directly reflects the number of macrocells contained in each part. Where common packages exist, both XC9500 and XC9500XL have the same functional pins, so legacy designs can be easily migrated from XC9500 versions to XC9500XL versions. The main changes are small, but important. First, a new FastCONNECT II Switch Matrix is introduced with more inputs per Function Block and greater speed. Second, Macrocell functionality is enhanced by adding clock enable capability. Third, an improved power up model makes interfacing with other chips even easier than before. Fourth, each macrocell can select the clock phase of any clock source - globals or product term, individually. Finally, this is all automatically supported with Xilinx Foundation and Alliance Design Software solutions making CPLD designs easier than ever before.

Function Block Interconnect

XC9500XL interconnect is performed by an extremely fast high speed multiplexer that connects all input pins and macrocell feedback points to Function Block inputs. An important fact about the interconnect is that all connections are uniform, and uniformly fast. This allows the XC9500XL to deliver a low power, fast and more flexible solution than any CPLD available.

Function Blocks

One factor that limits the ability of design software to fit designs is the number of inputs available for signals to gain entry into the CPLD Function Blocks. XC9500XL Function Blocks permit up to 54 signals to find entry sites. Once signals gain entry, the And Array portion of the Function Block can attach to whatever macrocells are needed.

The And Array contains ninety product terms that are assigned as needed by the design software which controls the Product Term Allocator. The software will direct product terms to macrocells to build the designer's functions with the number required for each macrocell. Up to ninety product terms can be assigned to a macrocell, if required. Macrocell outputs can be directed by the FastCONNECT II Switch Matrix to attach to output and / or feedback points. See Figure 2.

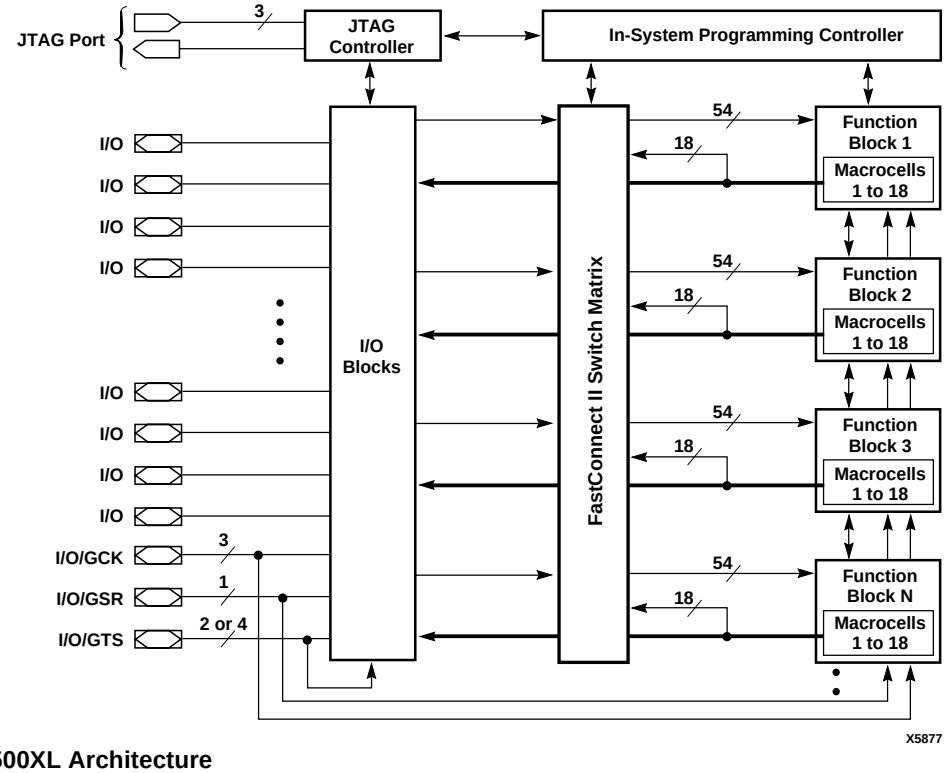

Figure 1: XC9500XL Architecture

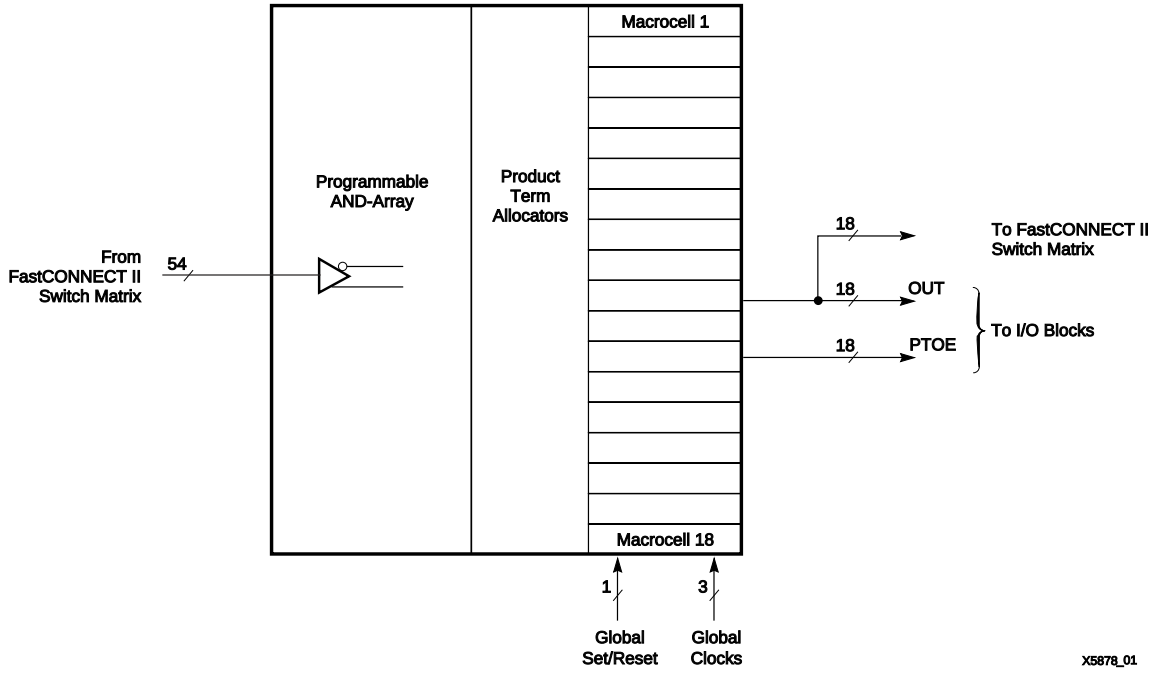

Figure 2: XC9500XL Function Block

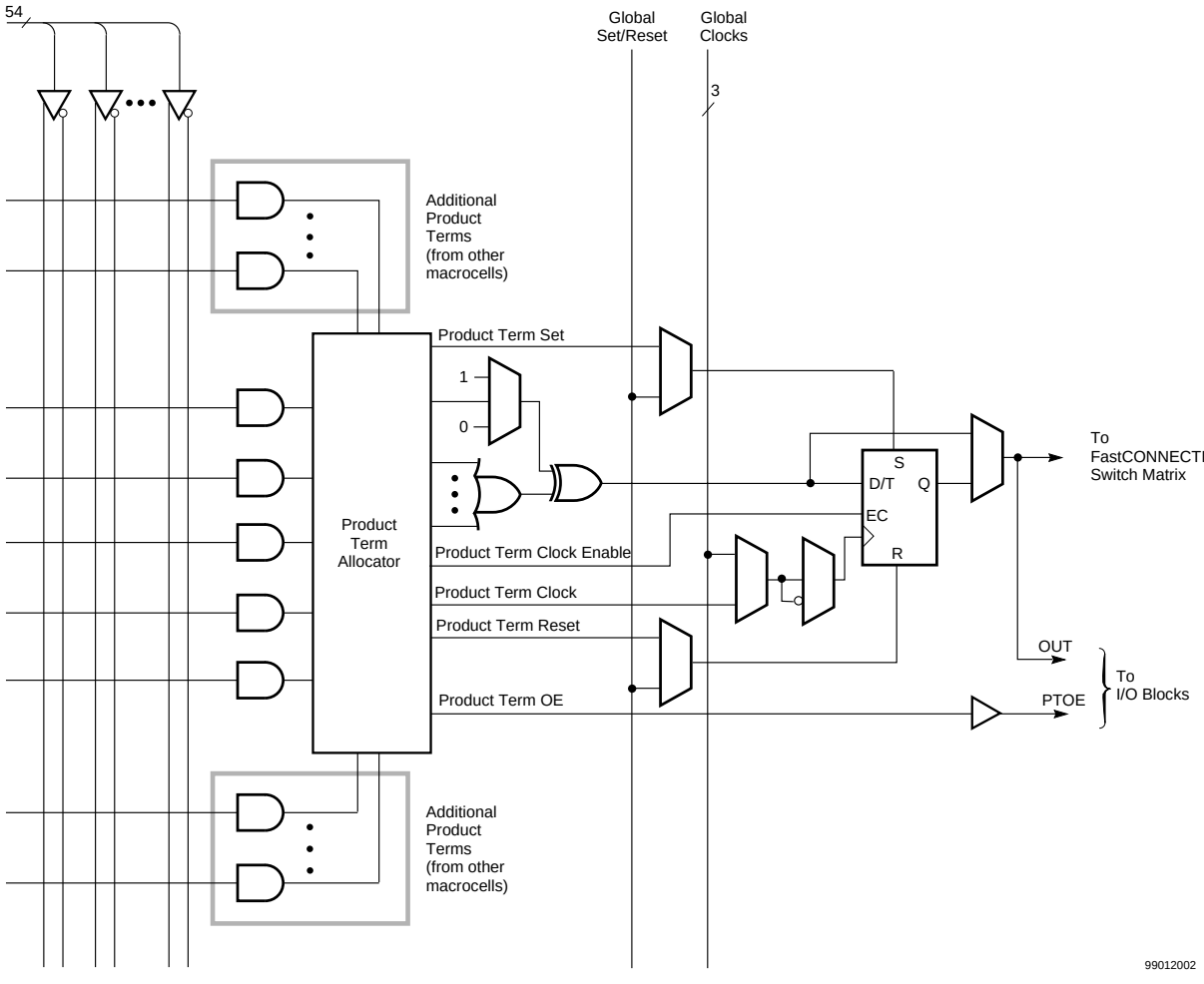

Figure 3: XC9500XL Macrocell

The Macrocell

In its native configuration, the XC9500XL macrocell (Figure 3) can be thought to have 5 product terms directly available to it. By appropriately importing unused neighboring product terms, the macrocell logic can “grow”. By exporting unused product terms to neighboring macrocells, the macrocell logic can “shrink”. Table 1 shows about how many product terms (P-Terms) are needed to form some common logic functions. When designing, this gives an idea of how many p-terms are used to create the various functions. Naturally, more operations exist than these, which can be found in the Xilinx Library documents.

As shown in Figure 3, the macrocell is comprised of the product term allocator, several configuration multiplexers and a D/T type flip flop with clock enable. The five native product terms can be thought of as directly available at this macrocell site. In the native condition, each product term can be thought of as having at least three alternate configurations.

Table 1: Macrocell/Product Term Usage

Data Operation	P-Terms Used
Shift Register	1 per bit
Counters	1 to 4 per bit
N:1 Mux	N
2-Bit Adder	6
Exclusive-OR	2
Storage Register	1

First, a p-term has a designated specialty function at a particular macrocell. This is the ability to form a product term output enable, a product term clock, a product term set, product term reset or drive one leg of the EX-OR gate. An alternate configuration for a product term is to participate in the local sum of products logic via the OR gate that drives one EX-OR input pin. If a product term does not contribute its specialty function at the macrocell, or participate in the local logic OR operation, then it is available to be collected by another OR and forwarded to a neighbor macrocell in either direction. This is termed cascading, and will be described in more detail later. Finally, the product term set

and reset product terms can assume the functionality of driving the flip flop clock enable. Figure 4 shows details of Product Term Allocation and Figure 5 and Figure 6 show how clock enable circuitry is created.

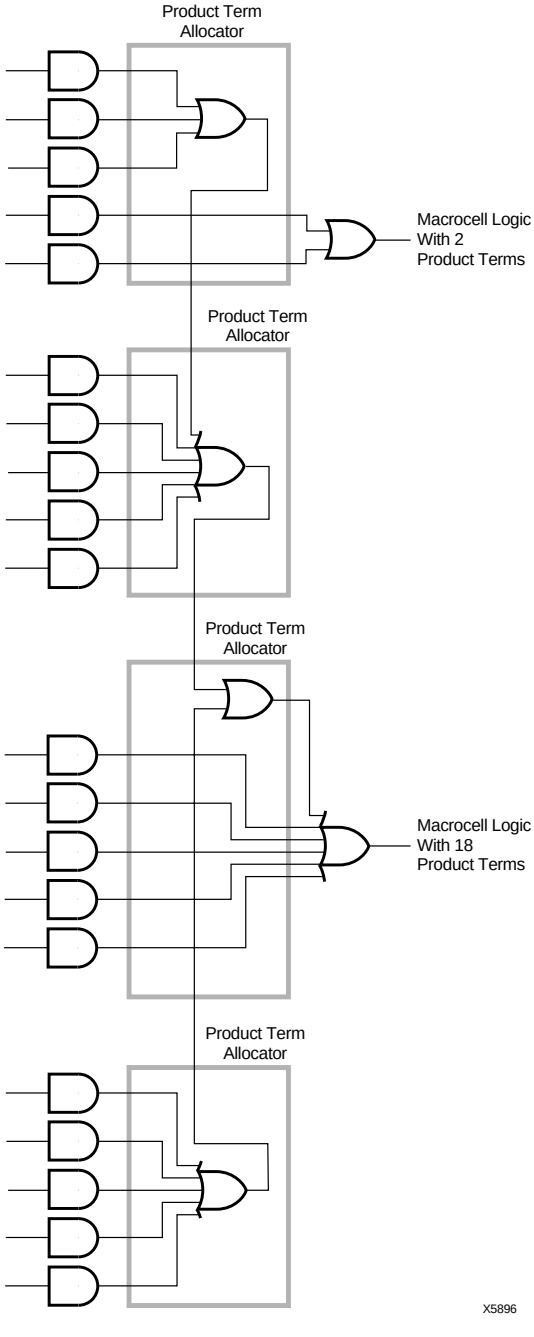

Figure 4: Product Term Allocation

In Figure 4, all but the Product Term Allocators have been omitted for clarity. In this situation, the design requirement is to deliver 18 product terms to the designated sum of product output site. The native set of 5 p-terms is supplemented with 5 p-terms from each directly adjacent neighbor taking the tally to 15 product terms. In this case, three more p-terms are needed, so the software must find them. The next site (to the north) requires two of its native 5 product terms, but three are available to meet the demand. The software forwards the available three p-terms to the required delivery site. In this case, two cascade times are required to provide 18 product terms. Note that the solution is not unique. The software could just as well encounter an adjacent neighbor with locked down product terms and been forced to skip over another macrocell to satisfy its need. The bidirectional cascade permits passing to/from both directions, which increases the likelihood of finding needed logic. This typically gives results within a single cascade and occasionally needs to go further. Product terms are located circularly so that the bottom macrocell can pass directly to the top macrocell and vice versa. An important factor here is that every macrocell has the same potential access to product terms.

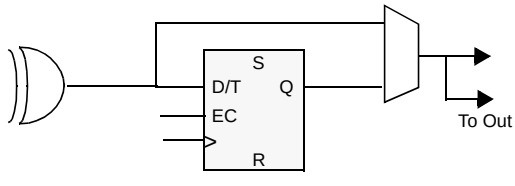

Figure 5: D/T Flip Flop Clock Enable Notation

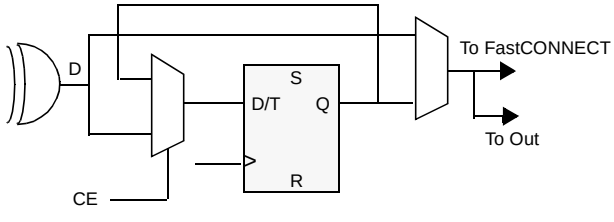

Figure 6: D/T Flip Flop Clock Enable Structure

In Figure 5, the Flip Flop shows separate D/T and EC (clock enable) pins attached to the flop. Actually, the term clock enable is a misnomer, because as shown in Figure 6, it is simply a mux select pin that chooses between an external “D” pin and the flop's own Q output. Clock enable does introduce an additional control pin to be managed, but is often used in cases where designers would otherwise be tempted to gate the clock to obtain design control.

Not emphasized in the macrocell diagram is the ability to selectively invert any clock entering the clock mux before attaching to the flip flop clock input point. Figure 7 details how this is achieved at every macrocell site.

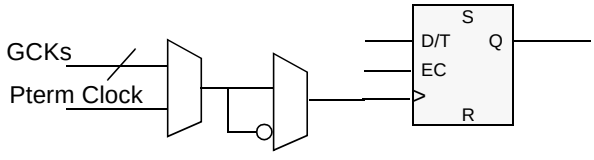

Figure 7: Macrocell Clock Inversion Selection

XC9500XL Pin Migration Capability

Table 2 shows the pin compatibility among XC9500XL devices. Designs can be easily migrated to larger and smaller devices. In many cases greater density with equivalent speed can be obtained by using larger parts. If a design is initially targeted to a smaller device, the same design can be easily moved into a larger device, if more capacity is required. This capability allows designers to maintain their pin assignments when designs must be moved to a larger device. Moving designs from larger to smaller devices can also be accomplished, while keeping the original pinout, if the smaller device has enough resources to contain the design.

A reasonable design practice would be to pick the lowest capacity for a given package in the slowest speed grade. Then, as design proceeds, larger or faster parts can accept the design as expectations and/or needs change. Picking the slowest and least dense part would economically be the best first choice, anyway. The key is to first pick the one closest to your needs. This approach would be somewhat different, if future field upgrade was a consideration, because here it might be appropriate to “over spec” a part to include speed latitude and additional available function for unforeseen future changes.

Table 2: XC9500XL Available Packages and Device I/O Pins

	XC9536XL	XC9572XL	XC95144XL	XC95288XL
44-Pin PLCC	34	34		
64-Pin VQFP	36	52		
100-Pin TQFP		72	81	
144-Pin TQFP			117	117
208-Pin PQFP				168
48-Pin CSP	36	38		
144-Pin CSP			117	
352-Pin BGA				192

XC9500XL Timing Model

The XC9500XL Timing Model is shown in Figure 8. This type of diagram exposes the architecture of an XC9500XL part in a way that each encountered time delay is shown. Table 3 summarizes the individual time delays found. The parameters identified in Table 3 are present in the fitter report for a particular design. This lets a designer identify exactly how their design's performance is determined by simply tallying the delays incurred as each signal visits the various internal part functions. For instance, tPD is determined in the simplest configuration as:

$$t_{PD} = t_{IN} + t_{LOGI} + t_{PDI} + t_{OUT}$$

Other paths are easily identified and more examples are provided in the XC9500XL Timing Application Note. (See Xilinx application note number *XAPP111 - Using the XC9500 Timing Model*.)

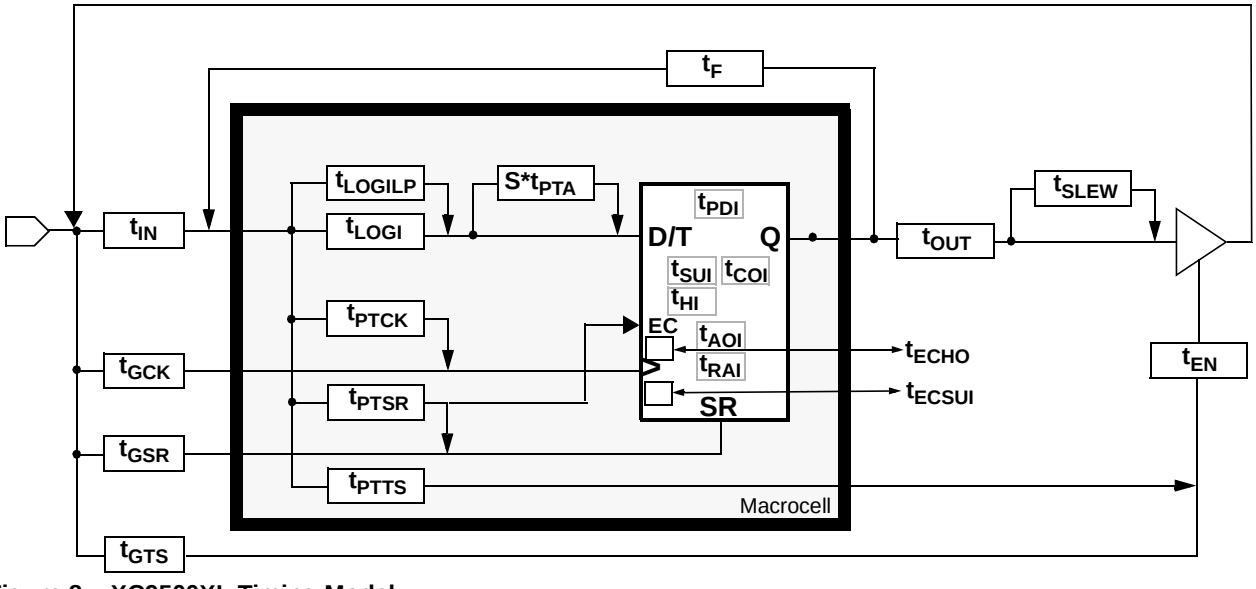

Figure 8: XC9500XL Timing Model

Table 3: Timing Parameters

Parameter	Name
t_{AOI}	Register asynchronous S/R to output delay
t_{COI}	Resister clock to output valid delay
t_{E}	Output tri-state enable time
t_{ECHO}	Enable clock hold time
t_{ECSUI}	Enable clock setup time
t_{GCK}	GCK buffer delay
t_{GSR}	GSR buffer delay
t_{GTS}	GTS buffer delay
t_{HI}	Register hold time
t_{IN}	Input buffer delay
t_{LOGI}	Internal logic delay
t_{LOGILP}	Internal low power logic delay
t_{OU}	Output buffer time delay
t_{PDI}	Combinatorial logic propagation delay
t_{PTA}	Incremental product term allocator delay
t_{PTC}	Product term clock delay
t_{PTTS}	Product term tri-state delay
t_{RAI}	Register asynchronous S/R recovery before clock
t_{SLEW}	Slew rate limited delay
t_{SUI}	Register setup time

Practical Considerations

Power On Model

XC9500XL parts are designed to provide a flexible voltage environment for today's demanding voltage environments. Key to this is considering lots of details that permit designers the choice of speeds and densities, but automatically handle electrical issues that are frequently overlooked by others. First on the list is a flexible "Power On Model". Figure 9 shows how an XC9500XL powers up. In this diagram, we will assume V_{CCINT} and V_{CCIO} are either tied together or rising together. In this case, as V_{CC} rises, the pins are assumed initially to be in high impedance condition, with large pullup resistance to V_{CCINT}. This provides a logic high that can be easily counter driven by a pin from an external chip wishing to dominate that electrical point. At one point in the power up process, the XC9500XL passes its internal configuration bits to the parts functional resources and the outputs are configured as dictated by the programming pattern. When the part is powered down, small keeper circuits retain the last value the pins drove as VCC drops. Some variation occurs if V_{CCIO} is cycled separately, but in all cases, the most benign electrical state is assumed.

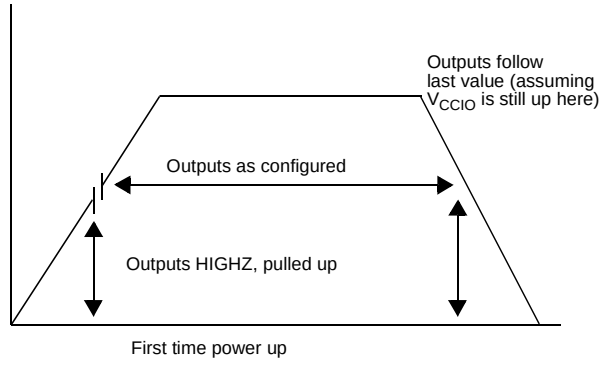

Figure 9: Power Up Model

Mixed Voltage Operation

XC9500XL I/Os are designed to deliver output signals that range from 0 to 3.3V (+/- 10%). Figure 10 details the separation between V_{CCINT} and V_{CCIO} and shows the CMOS output buffer. Figure 11 and Figure 12 show operation with mixed voltages. Table 4 summarizes the voltage compatibility of the XC9500XL and other logic families. Finally, Figure 13 shows the input hysteresis that improves noise margin for XC9500XL inputs.

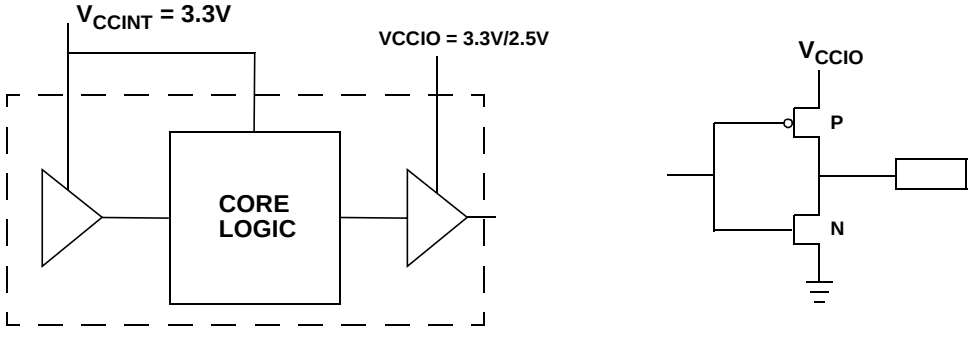

Figure 10: XC9500XL I/O Architecture and Output Structure

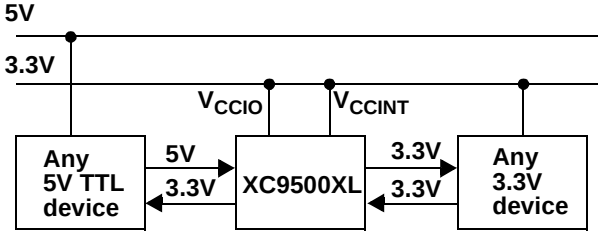

Figure 11: Mixed Voltage 3.3/5V Operation

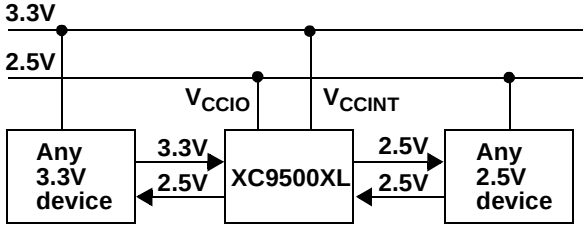

Figure 12: Mixed Voltage 3.3/2.5V Operation

Table 4: XC9500XL Voltage Compatibility Summary

	5V CMOS	5V TTL	3.3V LVCMOS	3.3V LVTTL	2.5V Normal
V_{IL}	X	X	X	X	X
V_{IH}	X	X	X	X	X
V_{OL}	X	X	X	X	X
V_{OH}	3.3V	3.3V	X	X	X

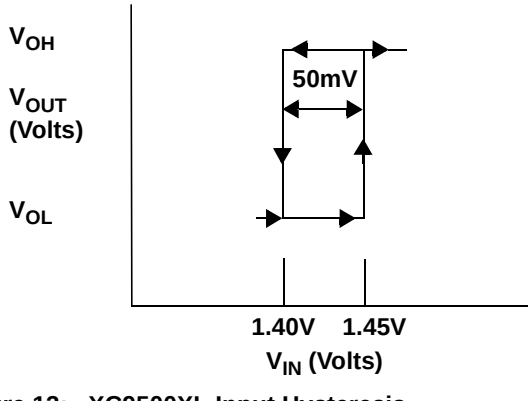

Figure 13: XC9500XL Input Hysteresis

Power Management Considerations

XC9500XL family parts provide substantial power reduction simply because the internal V_{CC} ranges well below that of 5V CPLD families. Due to the square law relationship, this alone provides a nearly 60% reduction in power over 5V families. However, internal options are provided to lower power even more. This includes the ability to operate each product term in a low power mode (at nominal speed reduction) and the ability to operate the I/O pins at 2.5V when appropriate.

Optimizing Power

The following guidelines will aid in reducing power consumed by an XC9500XL CPLD.

1. Terminate unused Input pins. This guarantees they are not floating. A convenient way to do this is with the User Programmable Ground (UPG) feature.
2. Assign High Speed only to those macrocells that absolutely require it. The remaining macrocells should be placed in low power mode.
3. Eliminate or minimize slow slewing input signals. These signals require input buffers to remain in their conducting region for long periods.
4. If possible, set V_{CCIO} to the 2.5V level to limit the output voltage swing range and lower power in that section.

Power Supply Sequencing

Separate power supplies for V_{CC} and V_{CCIO} may be powered up or down in any sequence without harming an XC9500XL CPLD.

High Speed Design Considerations

Although XC9500XL parts are not prone to having signal quality issues, ground rise and signal reflections can be managed by planning. The following design guidelines should strongly be considered in advance to avoid difficulty when operating with lots of simultaneously switching signals and at high frequencies.

1. Only connect the essential outputs to I/O pins. Intermediate shift register bits and counter bits that need not drive outputs should remain buried.
2. Minimize the number of outputs switching simultaneously.
3. Two global clock inputs can be managed by delaying one to introduce signal skew. Breaking long clock chains across multiple clock drivers can provide skew (less than 1 nanosecond) that can significantly reduce ground rise.
4. Using additional ground pins can lower ground rise effects. Unused pins configured as User Programmable Grounds (UPG) can be tied directly to the PCB ground plane. This splits the current driven into heavily loaded ground pins and lowers the voltage rise. Best UPG placement is uniformly around the chip, if possible.
5. Signal skewing can reduce ground rise. This can be achieved by mixing ordinary and fast slew rate outputs. Only assign fast slew rate to signals that require it.

PC Board Layout Considerations

Key to a good digital design is a good electrical design. The following checklist will be helpful to make sure practical oversights do not occur when creating a new printed circuit board. Most of these practices are typical of high speed microprocessor board design, so there should be no issue when using the same practices for XC9500XL CPLD designs.

Layout Checklist

1. Avoid floating inputs. Invoke User Programmable Ground if possible to deliver low driven output signal to internal input. For additional ground management, attach such pins to PCB ground.
2. Locate XC9500XL parts near the devices they drive (or are driven by) to minimize transmission line effects.Use wide spacing between fast signal lines (particularly clocks) to minimize crosstalk.
3. Place power pins (V_{CC} and GND) on separate board planes. Fast signals should reside on a different plane, still.
4. Decouple all device V_{CC} pins with 0.1 µF and 0.01 µF capacitors connected to the nearest ground plane. Low inductance surface mounted capacitors are recommended. Some designs may require different values.
5. Decouple the printed circuit board power inputs with 0.1 µF ceramic (high frequency) and 100 µF electrolytic (low frequency) filter capacitors.
6. Connect all device ground pins together, to ground.
7. Avoid using sockets to attach XC9500XL CPLDs to the PCB. Direct soldered connection minimizes inductance and reduces ground rise. XC9500XL CPLDs are specifically designed for direct PCB attachment.

Pin Preassigning Guidelines

Frequently, designers must layout their PCBs prior to the development of the design. Any commercially available CPLD will have difficulty keeping the pin assignment for a totally arbitrary design done with little or no forethought. As mentioned earlier, it is a good idea to always target a design to the lowest density available in a given package for the slowest speed grade available.

If a legacy design can be used as a “comfortable” model, then it's pin assignment may be appropriate. In this case, having density and speed slack available is important. If no legacy design exists, spreading the pins uniformly so that available blank slots exist between pins will help assure available product terms will exist to handle future changes as the design proceeds. Remember, pin preassigning without having the software make a first pin assignment is not recommended. If at all possible, let the design software have a preliminary version of the design prior to producing a printed circuit board, to assure a reasonable first pinout has been obtained.

Boundary-Scan and ISP Capability

XC9500XL CPLDs include a significant repertoire of IEEE std 1149.1testing and JTAG ISP instructions. Table 5 summarizes the set of instructions that might be encountered during a design. Others exist, which are proprietary to Xilinx CPLDs.

Table 5: Supported JTAG & ISP Instructions and Affected Registers

Instruction	JTAG Registers
Bypass	Bypass Register
Clamp	Bypass Register
EXTEST	Boundary Scan Register
FlashErase	Configuration Register
FlashProgram	Configuration Register
FlashVerify	Configuration Register
HIGHZ	Bypass Register
INTEST	Boundary Scan Register
Sample/Preload	Boundary Scan Register

Multi-voltage JTAG Capability

XC9500XL CPLDs are designed specifically to operate in a multivoltage JTAG environment and maintain full signal and JTAG integrity. Internal pullup resistors are on TMS and TDI to 3.3V.

ISP Checklist

When programming an ISP CPLD, best results are obtained when common practices are used. The following checklist gives the standard points to observe to obtain best ISP results.

1. Make sure V_{CCINT} is within the rated value: 3.3V +/- 5%.
2. Provide both 0.1 and 0.01 µF capacitors at every V_{CC} point of the chip, and attach directly to the nearest ground.
3. Use the latest Xilinx download cables. This would be a Parallel Cable with serial numbers greater than 5000 or any X-Checker cable.
4. Consider including buffers on TCK and TMS interleaved at various points on your JTAG circuitry to account for unknown device impedance.
5. Always be certain to use the latest version of the Xilinx JTAG Programmer Software.
6. Put the rest of the JTAG chain into HIGHZ when programming a troublesome part. This is optional.
7. If free running clocks are delivered into the ISP CPLD, it may be necessary to disconnect or disable their entry into the CPLD while programming.
8. For XC9500XL designs attach VCC from the parallel cable to 3.3V on the PCB.

Conclusion

XC9500XL CPLDs provide an abundance of logic resources and require only a minimum number of design considerations to obtain the best results. By carefully following the guidelines and checklists included here, designers can expect to obtain all the features needed in today's high speed, low voltage systems.