XILINX®

5 Volt Tolerant and PCI

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Summary

The purpose of this application note is to investigate the PCI (Peripheral Component Interface) environment when using 5V tolerant, 3.3V supply integrated circuits. In particular, we will examine the meaning of the statement "PCI compliant" when used in CPLD or FPGA data sheets.

5V Tolerance

When a silicon vendor offers a 5V tolerant part, the design group will put additional circuitry into each I/O cell to allow the pin, when used as an input, to go above the 3.3V V_{CC} rail. This circuitry can be fairly complex, typically involving more than a dozen transistors. The primary goal is to keep the output buffer's PMOS pull-up transistor from turning on. Without the extra circuitry there will be a leakage path (Figure 1) from the output pin through the PMOS transistor (in the reverse direction) back into the 3.3V supply. With the extra circuitry added (not shown here) the leakage will be limited to the parasitic leakage of a turned-off transistor, typically a few nanoamperes.

3.3V
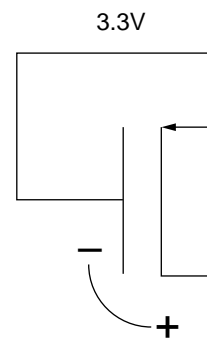
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Figure 1: **Circuit Leakage Path**

Precautions should also have been taken by the manufacturer to prevent any 5V signal from damaging the thin oxides that are typical to 3.3V processes. This requires either additional process steps or circuit design complexity. See the section on Silicon Reliability for 5V Tolerance for further discussion.

One thing is certain. Five volt tolerance is incompatible with any diode that points from the output pin back into the 3.3V supply, as shown in Figure 2. However, such a diode is required by the 3.3V PCI spec. This note will address the consequences of this conflict, with suggestions for addressing the issue in your board design.
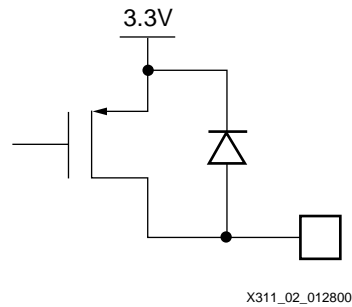
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Figure 2: **5V Tolerance Incompatibility**

3.3V PCI and Diode Clamping

The PCI electrical spec is defined in such a way as to provide open termination incident wave switching across a wide range of board impedances. It does this by defining minimum and maximum driving impedances for the ICs output buffers. The PCI specification also stipulates mandatory use of an input clamp diode to V_{CC} for 3.3V signaling. The reason for this is to ensure signal integrity at the input pin by preventing the resultant ringing on low-to-high edges from dipping below the switching threshold. To see this, consider the unclamped case, which is shown in Figure 3. A 3.3V output signal from a 10 ohm source impedance[1] into a 70 ohm transmission line will generate an incident wave voltage of 5.8V at the receiving end. After two flight delays, a negative reflected wave will follow, getting dangerously close to the upper end of the input threshold[2].
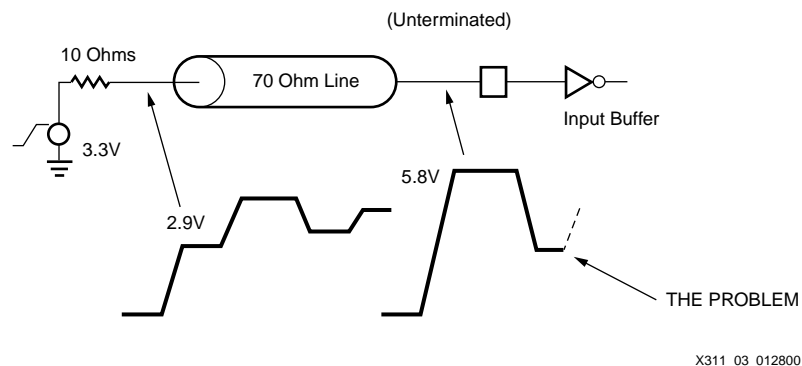

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Figure 3: **Unclamped Example**

(Although this discussion is aimed at PCI applications, note that the same issue can exist in any board design with open termination transmission lines.)

The overshoot voltage can be this high because the input buffer is an open impedance, due to its 5V tolerance. The addition of an external clamp diode to the 3.3V supply will dampen this overshoot and reduce the ringing sufficiently to avoid spurious threshold transitions.

It might occur to the reader that a programmable diode at each pin would be a nice feature on-chip. This has actually been implemented on at least one PLD. The PCI spec requires that the diode (and a series switching device) be able to pass a current of 25 mA with a forward drop of less than 1V. The silicon area required of such a diode and switch is roughly as large as the output buffer transistors, too large an area to justify except in special applications. (If these components are not used, the area must still be paid for.)

A 3.3V PLD which stipulates in its data sheet that it is "PCI complian" while also offering 5V tolerance is probably referring to the electrical drive characteristics of the output buffer. (The minimum and maximum source impedances referred to previously.) If a particular pin is used in a PCI environment, an external clamp diode will need to be added at that pin, for the reasons shown above.

5V PCI Singaling

It is also possible to consider use of 3.3V PLDs within a 5V PCI environment. Output buffers designed for 3.3V operation generally drive to the V_{CC} rail, and these can meet the PCI spec if the PMOS pull-up transistor is sufficiently large. The values of allowable drive impedances for both 3.3V and 5.5V signaling are shown in Figure 4 and Figure 5. (Note that the V_{CCIO} is 3.3V in both cases.)

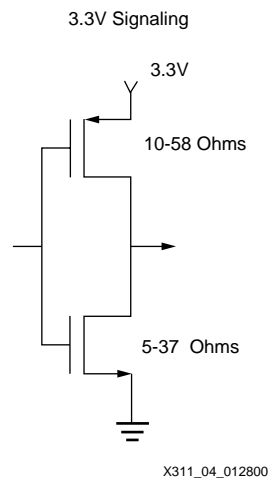3.3V Signaling

3.3V

10-58 Ohms

5-37 Ohms

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Figure 4: **3.3V Signaling**

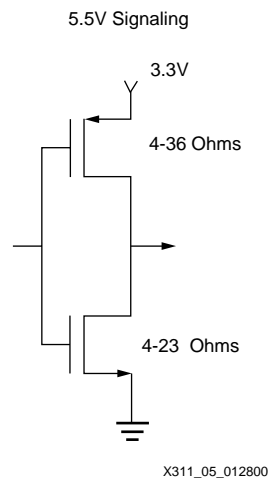5.5V Signaling

3.3V

4-36 Ohms

4-23 Ohms

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Figure 5: **5V Signaling**

As can be seen, there is sufficient overlap in the specification to make it feasible for an output buffer to be electrically compatible with both 3.3V and 5V PCI signaling. Note, however, that it is possible for a device to satisfy the 3.3V specification, but not have sufficient drive for the 5V signaling environment. The 3.3V component vendor should be clear when specifying PCI electrical compatibility as to the specific signaling environment(s) that it adheres to.

(It may seem strange that a 5V PCI signal can be driven with a 3.3V signal. However, the 5V PCI threshold was put at TTL levels (centered around 1.4V), with a 2.0V guaranteed high level. This permits a 3.3V output driver to interface to the bus, as long as the drive impedances are low enough.)

The PCI specification requires that a 5V PCI compatible device be able to withstand repeated application of 11V pulses sourced through a 22 ohm resistor without damage. For 5V tolerant pins, this mandates the use of an external clamp diode. The application of 11V to an unprotected I/O structure will cause damage.

The reason for this specification is that when a device receives a 5V PCI signal as an input (either to a dedicated input pin or to a 3-stated I/O pin) the PCI signal will, by design, overshoot to well above the 5V supply. Although "5V tolerant" parts can normally accept signals on the bus up to 5.5V (5V + 10%) the overshoot of an unclamped PCI signal can be well over seven volts. For this reason, a clamp diode must be added from the pin to the 5V board supply. Xilinx devices that are specified for 5V PCI signaling are able to withstand an absolute maximum voltage of 6.5V safely. This rating gives the margin needed to allow a diode forward voltage drop above the 5.5V supply. If a vendor specifies an absolute maximum on the input pins less than 6V, this is not high enough to give reliable operation in a 5V PCI signaling environment.

Silicon Reliability for 5V Tolerance

A 3.3V operation, 3-statable output buffer which does not have 5V tolerance will clamp at a diode above V_{CC} (see Figure 6). A 5V tolerant output structure in its most basic form includes a switch which allows the n-well of the PMOS output driver to follow the output pin voltage upwards. Additional circuitry is added to keep the PMOS transistor from turning on in the "upside down" direction when the output pin rises above V_{CC}. The equivalent circuit of the PMOS transistor when 5V is applied to the pin is shown in Figure 7. The transistor is off and there are no leakage currents.
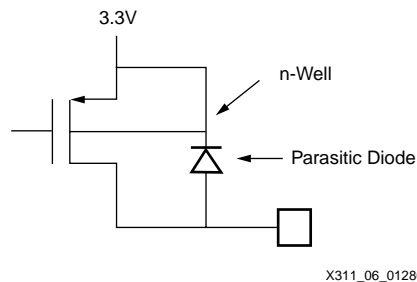

3.3V

n-Well

Parasitic Diode

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Figure 6: **Output Buffer without 5V Tolerance**
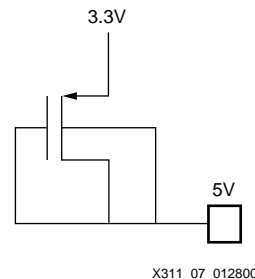

3.3V

5V

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Figure 7: **Equivalent PMOS Circuit**

There is an additional problem, however, that must be addressed by the PLD vendor. Take a look at a typical NMOS output structure shown in Figure 8. (The PMOS and its circuitry have been removed for clarity.) The 5V at the pin is a signal on the bus connected to this tri-stated output buffer.
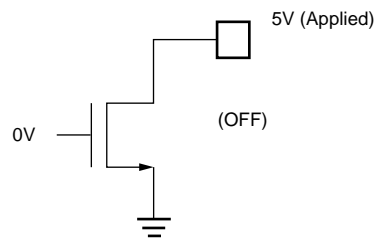

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Figure 8: **Typical NMOS Output Structure**

PLD devices which are targeted to the 3.3V market are currently manufactured with 0.35 micron technology. The wafer process used at this technology level will typically use a gate oxide thickness of 75 Angstroms (7.5 nm). Since the gate of the NMOS drive transistor is grounded to turn it off for 3-stating, the 5V at the output will appear across the drain-gate oxide region, creating a field of 6.7 MV/cm. The semiconductor industry has consistently kept CMOS operating voltages to around 5 MV/cm because of the damage that will occur to gate oxides at 7 MV/cm and higher[3]. In this case, 5V applied to the output pin (even though the pin is "5V tolerant") will come close to the critical value. Signal overshoot or supply voltage variation can easily cause this field to go higher. (The oxide degradation is cumulative, so short pulses over an extended time will eventually cause failure.)

The failure mode is not necessarily an oxide rupture. Injected charge trapped in the gate oxide can cause threshold shifts which gradually degrade the drive performance of the NMOS transistor, leading to slower speeds in the output buffer, especially with higher capacitive loads or (as in the case of this application note) in transmission line environments.

There are at least two approaches that the vendor can take to prevent this situation from occurring. One is to use a second, thicker, gate oxide for output transistors. This will lower the electric field to an acceptable level. (This particular approach is commonly used in 5V capable outputs, meaning the output buffer can actually drive 5V rail-to-rail signals by using a separate 5V I/O power supply.) However, the additional oxide step and associated masks add significant cost to the wafer, and this approach is usually not used for generating 5V tolerant circuits.

A second approach, and the one taken by Xilinx, is to add a second transistor in a cascade connection, with the gate connected to the 3.3V supply (see Figure 9). A thicker gate oxide is not needed, since the voltage across the gate is reduced. With the absolute maximum input voltage, 6.5V, that is specified with Xilinx devices (during the PCI 5V signaling overshoot condition), the voltage across the second transistor's drain-gate oxide region is only 3.2V, less than the part's normal supply voltage. It is apparent that if this 6.5V signal was applied to a single NMOS pulldown transistor (and assuming 75 Angstroms of gate oxide thickness) the field would be over 8 MV/cm. This is considered within the industry to be generally unacceptable.

5V (Applied)

3.3V — Cascade NMOS Transistor

0V — (OFF)
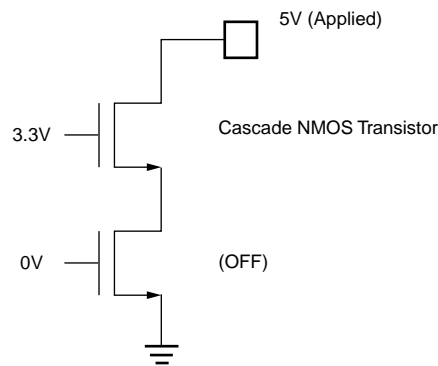
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Figure 9: **Cascade Connection**

Although the previous discussion looks specifically at a tri-statable output buffer, it should be noted that similar circuit techniques are needed in the input buffers. (For example, an input pin should not be wired directly to the gate of a grounded source NMOS transistor.) Xilinx PLDs have special circuitry at all input buffers to guarantee that the maximum field limits required by the process are not exceeded.

Conclusion

PCI electrical compatibility can be obtained with 5V tolerant, 3.3V operation, PLD devices. However, the manufacturer should explicitly specify compatibility with 3.3V and/or 5V signaling. In either case, the board designer is responsible for adding the necessary clamp diodes at the input and I/O pins. These clamp diodes are needed for:

- Signal integrity (3.3V signaling)
- Reliability (5V signaling).

Care should be taken by the vendor to ensure, either by process or design techniques, that the input and I/O pins are capable of withstanding the overvoltages expected in PCI environments.

References

1. *The 10 ohm value is from line CE26 of the PCI Electrical Checklist, Revision 2.1. This is the minimum allowed drive impedance.*

2. *The 3.3 volt PCI threshold spec is centered at 0.4 x VCC, ±0.1 x VCC.*

3. *See, for example, Chapter 4 of T. Hori, "Gate dielectrics and MOS ULSIs" Springer Verlag, N.Y., 1997.*

Revision History

The following table shows the revision history for this document.

Date	Version	Revision
02/14/00	1.1	Converted to Xilinx format.