Gate Count Capacity Metrics for FPGAs

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Summary

Three metrics are defined to describe FPGA device capacity: Maximum Logic Gates, Maximum Memory Bits, and Typical Gate Range. The methodology used to determine these values is described.

Xilinx Family

XC4000 Series, XC5000 Series

Introduction

Every user of programmable logic at some point faces the question: “How large a device will I require to fit my design?” In an effort to provide guidance to their users, Field Programmable Gate Array (FPGA) manufacturers, including Xilinx, describe the capacity of FPGA devices in terms of “gate counts.” “Gate counting” involves measuring logic capacity in terms of the number of 2-input NAND gates that would be required to implement the same number and type of logic functions. The resulting capacity estimates allow users to compare the relative capacity of different Xilinx FPGA devices.

In the tables in this document (and in the corresponding product specifications in the Xilinx *1996 Programmable Logic Data Book*), three metrics are supplied to measure the capacity of Xilinx FPGAs in terms of both gate counts and bits of memory, as shown in Table 1 and Table 2: “Maximum Logic Gates,” “Maximum Memory Bits” (only for FPGAs with on-chip memory capability), and “Typical Gate Range.” These tables also list the actual number of Configurable Logic Blocks (CLBs) or logic cells available in each device.

Maximum Logic Gates

“Maximum Logic Gates” is the metric used to estimate the maximum number of gates that can be realized in the FPGA device for a design consisting of *only* logic functions. (On-chip memory capabilities are not factored into this metric.) This metric is based on an estimate of the *typical* number of usable gates per configurable logic block (CLB) or logic cell multiplied by the total number of such blocks or cells. This estimate, in turn, is based on an analysis of the architecture of the logic block and empirical data obtained by comparing the implementation of entire system-level designs in the FPGA devices and traditional gate arrays.

The CLBs of the XC4000 Series devices each contain three function generators and two registers (Figure 1). Additional resources in the block include dedicated arithmetic carry logic. Using Table 3 as a guide, the potential gate count for a single CLB can be derived. (Table 3 lists the gate counts for a sampling of logic functions; these gate counts are taken directly from a typical mask-programmed gate array’s library.)

Table 1: XC4000 Series FPGA Capacity Metrics

Device	Number of CLBs	Max. Logic Gates (No Memory)	Max. Memory Bits (No Logic)	Typical Gate Range (Logic and Memory)
XC4003E	100	3K	3K	2K - 5K
XC4005E/XL	196	5K	6K	3K - 9K
XC4006E	256	6K	8K	4K - 12K
XC4008E	324	8K	10K	6K - 15K
XC4010E/XL	400	10K	13K	7K - 20K
XC4013E/XL	576	13K	18K	10K - 30K
XC4020E/XL	784	20K	25K	13K - 40K
XC4025E	1024	25K	33K	15K - 45K
XC4028EX/XL	1024	28K	33K	18K - 50K
XC4036EX/XL	1296	36K	42K	22K - 65K
XC4044XL	1600	44K	51K	27K - 80K
XC4052XL	1936	52K	62K	33K - 100K
XC4062XL	2304	62K	74K	40K - 130K

Table 2: XC5000 Series FPGA Capacity Metrics

Device	Number of Logic Cells	Max. Logic Gates	Typical Gate Range
XC5202	256	3K	2K - 3K
XC5204	480	6K	4K - 6K
XC5206	784	10K	6K - 10K
XC5210	1296	16K	10K - 16K
XC5215	1936	23K	15K - 23K

Table 3: Gate Counts for Some Common Logic Functions

Function	Gate Count
Combinatorial functions:	
2-input NAND	1
2-to-1 Multiplexer	4
3-input XOR	6
4-input XOR	9
2-bit carry-save full adder	9
Register functions:	
D flip-flop	6
D flip-flop with set or reset	8
D flip-flop with reset and clock enable	12

Table 4: Capacity ranges for XC4000 Series CLB Resources

CLB Resource	Gate Range
Gate range per 4-input LUT (2 per CLB)	1 to 9
Gate range per 3-input LUT	1 to 6
Gate range per flip-flop (2 per CLB)	6 to 12
Total gate range per CLB	15 to 48
Estimated typical number of gates per CLB	28.5

The function generators are implemented as memory look-up tables (LUTs); the F and G function generators are 4-input LUTs, and the H function generator is a 3-input LUT. Each LUT is capable of generating any logic function of its inputs; thus, in a given application, a 4-input LUT might be used for any operation ranging from a simple inverter or 2-input NAND (1 gate) to a complex function of 4 inputs, such as a 4-input exclusive-OR (9 gates) or, along with the built-in carry logic, a 2-bit full adder (9 gates). Similarly, the registers in the CLB account for anywhere from 6 to 12 equivalent gates each, dependent on whether built-in functions such as the asynchronous preset/clear and clock enable are utilized.

Thus, assuming that all three LUTs and both flip-flops are utilized, a single CLB may hold anywhere from 15 to 48 gates of logic (Table 4). Of course, in a given application, all the resources in every CLB will not be utilized. Using empirical data based on the compilation of system-level designs, the actual obtainable usage is estimated as about 28.5 gates per XC4000 Series CLB. For example, the XC4020E, with 784 CLBs, is rated with a capacity of 20,000 Maximum Logic Gates (784 x 28.5 = 22,344). (This factor is derated to 24 gates/CLB in the XC4025E device, as its utilization is somewhat limited by the available routing.)

Therefore, this metric is a “maximum” in that it assumes that every CLB is being used. Of course, this simple analysis does not take into account the many other logic resources available in the XC4000 architecture, including on-chip three-state buffers, global clock buffers, global reset, the registers and multiplexers in the I/O blocks, wide edge decoders, readback circuitry, and JTAG boundary scan test circuitry.

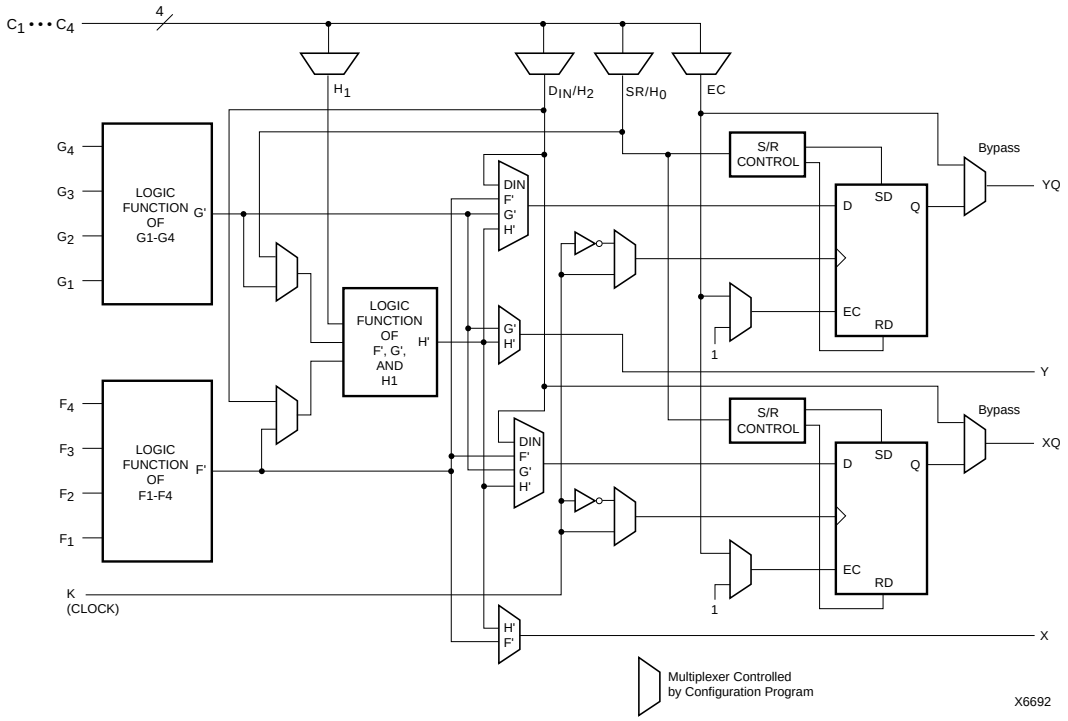
In the XC5000 Series architecture, each logic cell consists of a single 4-input LUT-based function generator, a register with built-in asynchronous clear and clock enable functions, and dedicated carry/cascade logic (Figure 2). (There are four such logic cells per XC5000 VersaBlock.) Thus, each logic cell is capable of implementing 8 to 21 gates of logic; empirical data based on the implementation of system level designs suggests an average of 12 gates per logic cell (Table 5). Thus, the “Maximum Logic Gates” capacity metric for the XC5000 FPGAs is 12 times the number of logic cells (or 48 times the number of VersaBlocks).

Maximum Memory Bits

Some FPGA devices, such as the XC4000 Series FPGAs, are capable of integrating RAM or ROM memory functions as well as logic functions on chip. This metric, quite simply, is the maximum number of memory bits that can be implemented on the device.

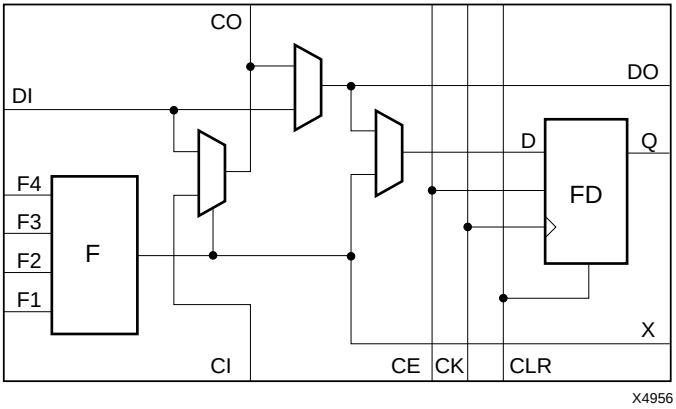
Table 5: Capacity Ranges for XC5000 Series Logic Cell Resources

Logic Cell Resource	Gate Range
Gate range per 4-input LUT	1 to 9
Gate range per flip-flop	7 to 12
Total gate range per logic cell	8 to 21
Estimated typical number of gates per logic cell	12



Note: The function generators and registers can be used together or independently. Dedicated carry logic is not shown.

Figure 1: Block Diagram of Logic Resources in the XC4000 Series Configurable Logic Block (CLB)



Note: one CLB contains four of these cells

Figure 2: Logic Resources in the XC5000 Series Logic Cell

In the XC4000 Series FPGAs, the F and G function generators optionally can be configured as a 32 x 1 or 16 x 2 block of asynchronous or synchronous RAM or ROM memory. Thus, for the XC4000 Series devices, this metric is equal to the number of CLBs multiplied by 32.

Typical Gate Range

FPGA users should realize that there can be considerable variation in the logic capacity of a given FPGA device dependent on factors such as how well the application's logic functions match the architecture of the FPGA device, the efficiency of the tools used to synthesize the logic and map, place, and route the device in the FPGA, and the skill and experience of the designer. For example, a given design is unlikely to use every available CLB or logic cell. For this reason, the "Maximum Logic Gates" metric is complemented with a "Typical Gate Range" estimate. Based on empirical data, this metric is intended to set realistic expectations by providing both a "low end" and "high end" estimate of FPGA capacity.

The "low end" of the Typical Gate Range for the XC4000 and XC5000 Series devices is calculated assuming about 2/3 of the "gate count per logic block" used to derive the Maximum Logic Gates; that is, about 18 gates per CLB for the XC4000 Series devices, and 8 gates per logic cell for the XC5000 FPGAs.

For the XC5000 Series FPGAs, the "high end" of the Typical Gate Range is just the Maximum Logic Gates metric described above. The XC4000 architecture allows the on-chip integration of memory as well as logic functions; the high end of the "Typical Gate Range" metric for XC4000 Series FPGAs assumes that a percentage of the device's resources are used for memory functions, as described below.

On-Chip Memory and the Typical Gate Range

Memory as well as logic functions can be integrated on an XC4000 Series FPGA, and the Typical Gate Range capacity metric takes this capability into account. In a sea-of-gates gate array, memory functions require about 4 logic gates per bit of memory. Thus, each XC4000 Series CLB is capable of implementing 32 x 4 = 128 "gates" of memory functions.

Most large system-level designs will include some memory as well as logic functions, and it is reasonable to assume that some memory functions would be implemented on an XC4000 Series FPGA in the typical system (especially for the larger devices in the series). For the XC4000 Series FPGAs, the low end of the "Typical Gate Range" assumes that all the CLBs are used for logic, with a utilization of about 18 gates/CLB. The high end of the "Typical Gate Range" assumes between 20% to 30% of the CLBs are used as memory (as delineated in Table 6), and the remaining CLBs are used as logic, with 128 gates/CLB for memory functions and 26 gates/CLB for logic functions. For example, assuming 20% of the 100 CLBs of the XC4003E are used for memory and the remaining 80 CLBs are used for logic, the high end of the Typical Gate Range is (20 x 128) + (80 x 28.5) = 4840 gates. The results of these calculations are rounded in Table 1 and Table 6.

Using Gate Counts as Capacity Metrics

Since the metrics used to establish gate counts are fairly consistent across Xilinx product families, these metrics are useful when migrating between Xilinx FPGA families, or when applying the experience gained using one Xilinx family to help select the appropriately-sized device in another family. The gate count metrics also are a good indicator of relative device capacities within each FPGA family, although comparing the number of CLBs or logic cells among the members of a given family provides a more direct measure of relative capacity within that family.

Unfortunately, claimed gate capacities are not a very good metric for comparing the density of FPGAs from different vendors. There is considerable variation in the methodologies used by different FPGA manufacturers to "count gates" in their products. A better methodology for comparing the relative logic capacity of competing manufacturers' devices is to examine the type and number of logic resources provided in the device.

Footprint Compatibility Lessens Risk

Designers do not always "guess right" when initially selecting the FPGA family member most suitable for their design. Thus, "footprint compatibility" is an important feature for maximizing the flexibility of FPGA designs. Footprint compatibility refers to the availability of FPGAs of various gate densities with the same package and with an identical pinout. When a range of footprint-compatible devices is available, users have the ability to migrate a given design to a higher or lower density device without changing the printed circuit board (PCB), thereby lowering the risk associated with initial device selection. If the selected device turns out to be too small, the design is migrated to a larger device. If the selected device is too big, the design can be moved to a smaller device. In either case, with footprint-compatible devices, potentially expensive and time-consuming changes to the PCB are avoided. Footprint compatibility has been incorporated in all Xilinx component product lines.

Summary

Xilinx derives its "gate count" capacity measurements using an extensive suite of actual system-level designs. These metrics represent typical utilization levels, with consider-

able variation dependent on the type of application. Users are invited to use similar methodologies to develop their own capacity metrics based on their own experiences and application needs.

Of course, many additional factors beyond capacity determine the effectiveness of a given FPGA in a given application, including performance, price, packaging, availability, power consumption, reliability, and ease-of-use.

Table 6: XC4000 Series FPGA Capacity Metrics showing Memory Usage Assumptions

Device	Number of CLBs	Max. Logic Gates[1] (No Memory)	Min. Logic Gates[2] (No Memory)	Max. Memory Bits (No Logic)	Typ. Memory Utilization (% of CLBS)	Typ. Memory Utilization (No. of CLBS)	High End of Typical Gate Range (Logic and Memory)
XC4003E	100	3K	2K	3K	20%	20	5K
XC4005E/XL	196	5K	3K	6K	20%	39	9K
XC4006E	256	6K	4K	8K	20%	51	12K
XC4008E	324	8K	6K	10K	20%	64	15K
XC4010E/XL	400	10K	7K	13K	25%	100	20K
XC4013E/XL	576	13K	10K	18K	25%	144	30K
XC4020E/XL	784	20K	13K	25K	25%	196	40K
XC4025E	1024	25K	15K	33K	25%	256	45K
XC4028EX	1024	28K	18K	33K	25%	256	50K
XC4036EX	1296	36K	22K	42K	25%	324	65K
XC4044XL	1600	44K	27K	51K	25%	400	80K
XC4052XL	1936	52K	33K	62K	25%	484	100K
XC4062XL	2304	62K	40K	74K	30%	691	130K

Notes:
1. Maximum Logic Gates calculated as number of CLBs multiplied by 28.5 gates/CLB (except XC4025E at 24 gates/CLB)
2. Minimum Logic Gates calculated as number of CLBs multiplied by 18 gates/CLB (except XC4025E at 15 gates/CLB)
3. All gate count figures are rounded
4. The fourth and eighth columns provide the lower and upper boundaries of the “Typical Gate Range” shown in Table 1.

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