DSP Design Tools
for Xilinx FPGAs

by Nick Lethaby, Director of Business Development, Elanix, Inc., nick@elanix.com

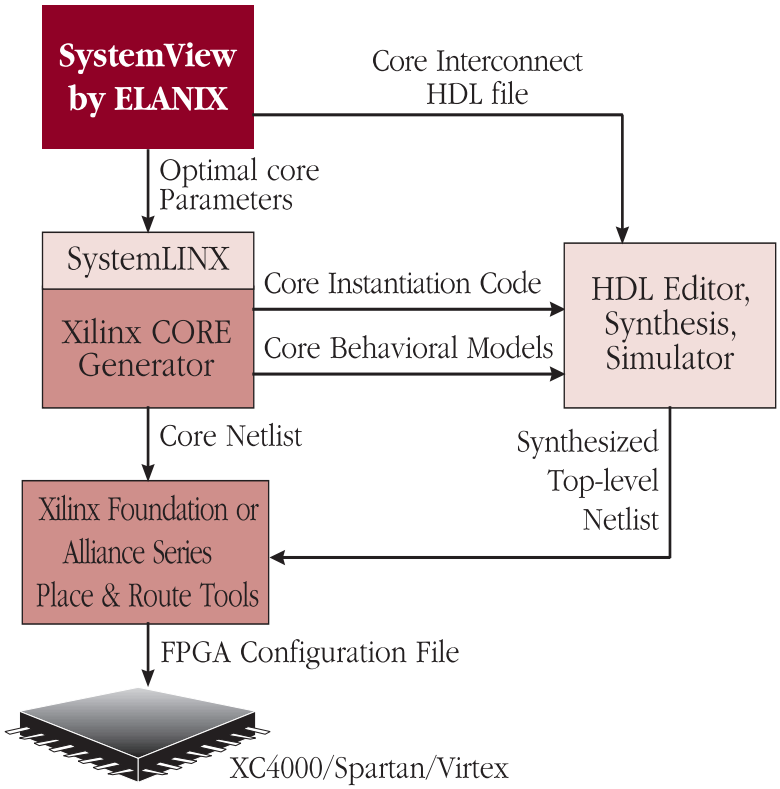
Over the past year, Xilinx has simplified the task of implementing DSP functions in FPGAs through the release of its optimized DSP LogiCOREs and its CORE Generator technology. Many users have experienced significant gains in productivity when using these DSP cores, because they no longer have to implement functions such as FIR filters from the ground up.

In a core-based design methodology, an efficient implementation is dependent on identifying the optimal parameters for a core. For example, a core that is programmed to use a 16-bit data path will use many more gates than a core employing only a 9-bit data path. Furthermore, even without bit-width optimization, DSP function design already involves significant complexity such as calculating the number of taps or determining coefficient values for a filter. Without access to a tool specifically designed for optimizing DSP functions, it may be extremely difficult to develop an efficient final silicon implementation.

System-level design tools that support the design of DSP functions have existed for some time. However, the traditional offerings in this arena have had a number of drawbacks. Some system design tools only effectively enable DSP function development using single- or double-precision floating point arithmetic. The digital designer is left with the difficult task of converting this design into fixed-point integer arithmetic using as few bits as possible. Although some tools have supported fixed-point and bit-width optimization, these have been not only very expensive but also very difficult to use.

During an evaluation of DSP system-level design tools, Ken Chapman, a Xilinx Applications Specialist focusing on DSP, identified SystemView by Elanix as a good system-level design solution for FPGA implementations. Chapman has found that digital designers tasked with doing DSP designs often lack a formal background in DSP theory. When combined with the lack of tools, it was clear that many engineers had little chance of producing a truly optimal design. "As a digital design engineer who lacked a strong mathematical background, I found SystemView enabled me to grasp key DSP concepts in minutes," stated Chapman, "In addition, SystemView was the only tool that combined ease-of-use with the sophistication needed for today's designs."

SystemView is integrated with the Xilinx DSP tools, providing a smooth flow from system-level design to silicon implementation.



Integration with the Xilinx DSP design flow

To further enhance SystemView for FPGA users, Xilinx and Elanix have integrated SystemView with the Xilinx DSP LogiCORE functions and CORE Generator.

Each Xilinx DSP LogiCORE, such as a FIR filter or multiplier, has a corresponding token in SystemView's DSP library. SystemView includes Xilinx-specific parameter checking to verify that the token parameter values are supported by the

> *"You can now use a visual design environment to directly generate high performance silicon implementations for DSP applications."*

actual LogiCORE core. Once the design is completed in SystemView, you can automatically invoke and pass core parameters to the Xilinx CORE Generator. The CORE Generator then produces netlists of the fully parameterized cores, HDL simulation models, schematic symbols, and HDL instantiation code.

In future releases, SystemView by Elanix will produce structural VHDL code, detailing the interconnectivity between the cores required to implement the whole DSP subsystem. This structural VHDL includes the instantiation code produced by the CORE Generator for each core. SystemView will automatically invoke the Xilinx Foundation VHDL editor so you can integrate the DSP subsystem with the remainder of the design.

About SystemView

SystemView consists of a core tool that combines design entry, simulation, analysis, and filter design. In addition, a range of optional token libraries are available. Users of Xilinx DSP solutions must obtain the core SystemView tool and the DSP library, along with a Xilinx FPGA option.

Some of the more important benefits of SystemView for designers of DSP and communication applications are briefly summarized below:

- **Faster design iteration:** You can build models using high-level functional blocks (tokens), without needing to worry about low-level details such as clocking. Compared to traditional block-diagram tools, SystemView's parameter inheritance capabilities greatly reduce the number of parameters that must be entered for each. Since simulation occurs at the algorithmic level, simulation speed is orders of magnitude greater than HDL simulators. As a result of these attributes, you can build, evaluate, and change models very quickly and rapidly explore different design options.
- **Bit-true DSP token library:** When using an FPGA, you can reduce the final gate count by using only the minimal number of bits required to maintain signal integrity. The SystemView DSP library provides bit-true DSP function simulation, including quantization to the exact arithmetic mode. This enables quick determination of the appropriate bit-widths without the need to develop bit-true C models or hardware prototypes.
- **Token libraries:** In addition to a bit-true DSP library, SystemView provides CDMA/IS-95, communications, RF/Analog, and TTL logic libraries. If desired, you can build end-to-end communication systems. In addition, mixed-mode behavior, such as an FPGA-based DSP function interfacing to an A/D, can be modeled up-front, reducing the likelihood of encountering unexpected problems later in the design cycle.
- **Analysis tools:** Tools such as HDL simulators do not provide adequate signal analysis. As a result, you may have to write custom programs to plot numbers in a meaningful way. SystemView provides a range of analysis tools specifically designed for signal analysis. These tools enable you to quickly produce meaningful data plots ranging from power spectrums to QAM constellations or phase locked loop phase planes.

Conclusion

This integration of SystemView by Elanix and the Xilinx CORE Generator provides a faster and simpler method for designing high-performance DSP applications. You can now use a visual design environment to directly generate high-performance silicon implementations for DSP applications.

For further information on Elanix and its products, visit the Elanix website at: www.elanix.com or call 818-597-1414. ◆

ELANIX INCORPORATED

**The term 'SystemView' is used as a shorthand form for SystemView by Elanix*