Concept® HDL
New Standard in Schematic Capture

Concept HDL replaces SCALD, adding many new features for FPGA design.

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Cadence Design Systems has introduced Concept HDL, a new HDL-based design creation tool to replace the older SCALD-based system. SCALD is a proprietary format that offered many advantages in its time, but now yields to the future. Concept HDL, based on the industry standards Verilog-HDL or VHDL, offers all the capabilities of its predecessor and in the PE13.5 release offers many new features that are essential for FPGA designs including support for the new Virtex family from Xilinx.

Enter Concept HDL

The HDL-centric data model upon which Concept HDL is built provides well-defined industry standards for expressing design structure, configuration, expansion, inheritance, scoping, constraints, and property annotations. The use of the standard also provides for easy third-party tool integration and a tighter, more natural union with simulators like the Verilog®-XL simulator, NC Verilog® simulator, Leapfrog® simulator, or Affirma™ NC VHDL simulator.

Concept HDL also features the new Occurrence Property File (OPF) that supports the proper reuse of hierarchical logic blocks. In this way, redundant logic does not need to be duplicated in the design, but is merely referenced as many times as needed. The OPF keeps separate property annotations for the different instances of reused logic but permits proper design expansion to either an FPGA or PCB design.

Concept HDL also offers the On-Line Electrical Connectivity Server (OLECS), a new feature that expands the design to a fully evaluated state for a variety of analyses or electrical rule checks. OLECS gives Concept HDL an understanding of the complete design, and moves it out of the realm of schematic capture into design creation. Combine the OPF and OLECS features together and you begin to understand what a step forward Concept HDL offers you.

Concept HDL and FPGA Design Creation

Concept HDL supports top-down, mixed-level, and bottom-up FPGA design flows. For the top-down and mixed-level flows Concept HDL is integrated with Synplify from Synplicity for design synthesis. Concept HDL writes Verilog and VHDL directly from a block diagram schematic that is defined in either Verilog or VHDL. The design is used by Synplify to synthesize the structural netlist that can be passed to the Xilinx place and route tools. This combination of high-level block diagram definition in Concept HDL and synthesis in Synplify make a powerful FPGA top-down design environment.

A mixed-level design consists of modules in Concept HDL defined in FPGA vendor primitives as well as modules that are described using Verilog or VHDL. Concept HDL can also treat modules as black boxes for designs where the FPGA layout or synthesis is complete and should not be redone. The top-down and mixed-level flows feature a tight integration between Concept HDL and Synplify that includes generation of Synplify project and constraint files. This provides Concept HDL with the ability to pass constraints to the synthesis engine to control the way the design is implemented in the physical device.

The End of SCALD as You Know It

With the future of design safely established with Concept HDL, the SCALD architecture will no longer be available. Cadence Design Systems, Inc. has offered all of its customers who are using the SCALD architecture a no-charge migration to the new HDL solution. As previously mentioned, in the PE 13.5 release Concept HDL also provides support for the Xilinx Virtex technology, which is not supported by SCALD. In fact, neither Xilinx nor Cadence Design Systems, Inc. will support the SCALD architecture with new technology, so now is the time to make the switch.

For more information about the powerful features of Concept HDL, or to learn more about the transition from SCALD to HDL, please visit the Cadence website at www.cadence.com. Registered users of Cadence tools may also visit SourceLink for more information on the transition.