Managing the Design Process with

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With Xilinx and third-party intellectual property (IP) companies providing solutions through the Xilinx LogiCORE and AllianceCore programs, you now have the choice of making or buying functionality for your designs. This has created a situation where various design sources may reside inside a single high-density FPGA.

For example, you may have a top-level schematic tying all of your underlying macros together. These macros may consist of blocks of purchased IP, in-house VHDL and Verilog, and even some schematic primitives. When combining these various design sources with a gamut of entry, synthesis, and verification tools, developing a workable design flow becomes an overwhelming task, and that's where IntelliFlow from Viewlogic becomes extremely useful.

For example, assume that you have a design that has a top-level schematic with underlying VHDL and Verilog blocks. When you are ready to take this design through place and route and back into your simulation environment for verification, you will probably come across the following set of issues:

- How do I synthesize my language macros and integrate these with my schematic?
- What options do I choose in the place and route tools so that I get the correct netlist out for verification?
- I'm targeting a device in a BG560 package. How am I going to create a 560 pin symbol with all of my power, ground, no connect, and programming pin information to use on my board design?

IntelliFlow,™ which is part of Viewlogic's Workview Office ® suite of tools, is a turnkey process manager for the design of complex programmable devices. The purpose behind a process manager like IntelliFlow is to take care of these issues for you. This way you can concentrate on the design without spending time on the interface details.

With IntelliFlow, you can mix schematics, VHDL, Verilog, and blocks of IP to generate high-quality results for your Xilinx FPGAs and CPLDs. IntelliFlow understands the mixed formats of the source files in your design and automatically configures tool flows to make the proper conversions between formats automatically, allowing you to focus on the design and not the interaction of tools.

For language-only or mixed language-schematic designs, the types of tasks supported by IntelliFlow are:

- Functional Simulation
- Synthesis
- Place and Route
- Timing Simulation
- Bit and PROM File Creation
- Automatic Board-level Symbol Creation

With the IntelliFlow process manager, the first step in doing a Xilinx design is to add your design source. In the example case of a block-level diagram with underlying language blocks, you would add your top-level schematic. IntelliFlow will parse and extract the design hierarchy for you, recognizing the VHDL and Verilog blocks and automatically pulling the necessary source files into the design process.

The second step is to pick your family, die, package, and speed that you are targeting. IntelliFlow has a database that contains all of the dies, packages, and speeds that are available for Xilinx, including the new Virtex family. By allowing you to select the die, package, and speed

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Viewlogic's IntelliFlow

individually, IntelliFlow protects you from picking an invalid combination.

The third step is to pick the type of simulation that you are planning on performing. If you have written a test fixture or testbench, you would select Verilog simulation or VHDL simulation respectively. On the other hand, if you are a user of Viewlogic's ViewSim™ gate-level simulator, you would choose gate-level simulation. At this point, IntelliFlow will take your schematic, create an EDIF netlist, and feed this EDIF netlist along with the underlying language blocks into FPGA *Express*™ for synthesis. This saves you from having to reformat your design manually and invoking multiple point tools.

With the design loaded in FPGA *Express*, you are ready to synthesize, place and route, and simulate. To perform these three steps, you just double-click on the Implement and Perform Timing Simulation tool. That's it. Behind the scenes, IntelliFlow will run FPGA *Express*. The netlist created by FPGA *Express* is fed into the Xilinx Alliance Series place and route tools. Since you have already chosen your simulation methodology, the correct Xilinx tools are run so that you get a VHDL, Verilog, or EDIF netlist that can be simulated. The netlist is translated, compiled, and loaded into the correct simulator.

When it is time to do board-level verification or layout, you just double-click on the Implement and Create Board Level Symbol Process. This process has many tools in common with the simulation process. Because of this, IntelliFlow knows not to re-run synthesis and place and route, which saves you time. Instead, it quickly takes the files that have already been created by the Xilinx Alliance tools and creates a symbol, on the fly. This symbol not only contains the pins that you have defined in your design, but power, ground, no connects, package information, and attributes that point to the underlying model for board-level simulation.

Although IntelliFlow handles the interactions of the various tools used in the design process behind the scenes, there is no loss of power for the Xilinx user. With IntelliFlow, you have *full* control over all of the tools used in the design flow. This includes the Viewlogic as well as the Xilinx tools. For example, if you are used to entering design constraints with the FPGA *Express* Timing and Constraint Editor, this editor is available to you via IntelliFlow. If you need to use the EPIC Design Editor or Xilinx Floorplanner, you can launch these from IntelliFlow. Individual settings for all of the Xilinx Alliance place and route tools are accessible. With context sensitive help, explanations for all of these tool settings are only a click away.

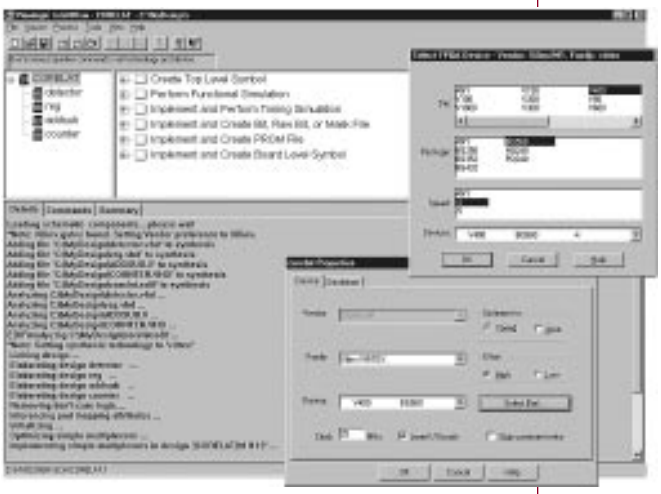

Figure 1: IntelliFlow Targeting the Xilinx Virtex Family

Conclusion

IntelliFlow provides a single graphical user interface for controlling design entry, functional simulation, synthesis, place and route, timing simulation, and board-level symbol creation. IntelliFlow performs data format changes automatically and runs the specific tools with the correct parameter settings for each of the Xilinx technologies. Full control over all of the Xilinx implementation tools is available through the IntelliFlow interface, giving you a combination of ease of use without loss of power. With IntelliFlow, you can focus on your design without having to deal with details of each tool used in the process or to learn new, complex design flows, reducing design errors and shortening your product development cycle.

For more information on the Viewlogic solution for FPGAs and other types of programmable devices, contact Viewlogic at 1-800-873-8439 or visit our website at www.viewlogic.com.