CMOS I/O Characteristics

by PETER ALFKE ◆ (peter@xilinx.com)

This article will give you an overview of our device I/O characteristics, to help you create better, more reliable designs.

All Xilinx devices use CMOS technology, which means there are two types of transistors:

- N-channel transistors, turned on by a positive gate voltage.
- P-channel transistors, turned on by a negative gate voltage.

For either transistor, the turn-on voltage must exceed the ~1-V threshold voltage.

Figure 1 shows a complementary inverter, consisting of a p-channel pull-up transistor and an n-channel pull-down transistor with both gates driven in common.

Outputs

All Xilinx devices, except for the XC9500 family and the original XC4000 family, have complementary outputs. However, for XC4000E, XC4000EX, and Spartan families, you must specify this option explicitly. The default on these devices is "TTL output" as described below.

Complementary outputs *(See **Figure 1.**)* are pulled "rail-to-rail," maximizing the output swing, especially desirable when driving other CMOS logic. With no DC load, the output voltage swings precisely between ground and Vcc with no voltage drop (the device output specifications of 0.4 and 3.86-V refer to particular dc loading conditions).

"TTL outputs" *(See **Figure 2.**)* have a reduced voltage swing, which achieves faster performance, especially for the High-to-Low transition when measured at the usual 1.5-V level. The term "TTL output" is actually a misnomer, derived from the similarity with the "totem-pole" structure of bipolar TTL outputs that use only npn transistors for pull-down and pull-up. Similarly, the "TTL output" structure in CMOS uses only n-channel transistors for pull-down and pull-up. This reduces the output High voltage (V_{oh}) by one threshold voltage, (1 to 1.5-V) below Vcc.

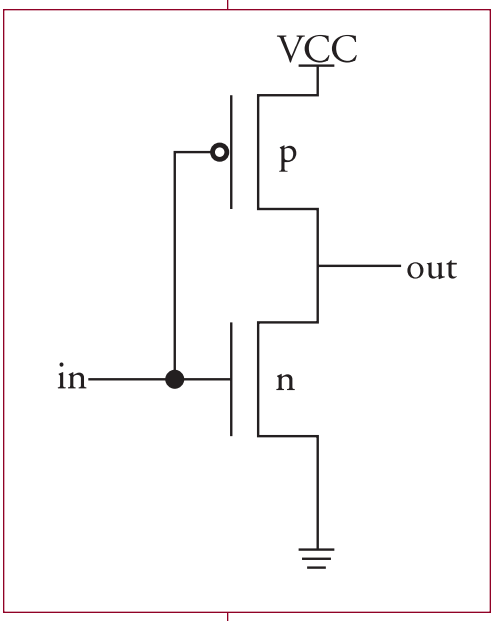
At 3.3-V supply voltages (and lower), complementary "rail-to-rail" or CMOS is the only available (and meaningful) output option.

The output impedance for our FPGAs is 15 to 30 Ω in the Low state, and 30 to 50 Ω in the High state. The output impedance for our XC9500 CPLDs is 10 to 12 Ω in the Low state, and 70 to 120 Ω in the High state

The XC9500 and the original XC4000 devices have TTL-level outputs only. On XC4000E, XC4000EX, and Spartan devices, TTL-output is the default, but can be changed to complementary output. If any data sheet specifies V_{OH} as >3.5-V, it is a complementary output. If V_{OH} is specified as 2.4-V, it is a TTL-level output.

Note that an output driving a long interconnect line or PC board trace can see reflections that drive the output well above Vcc and well below ground. Such reflections usually last for just a few nanoseconds (<10 ns) and are usually suppressed by the ESD protection diodes.

Figure 1.
Complementary Inverter or Buffer.



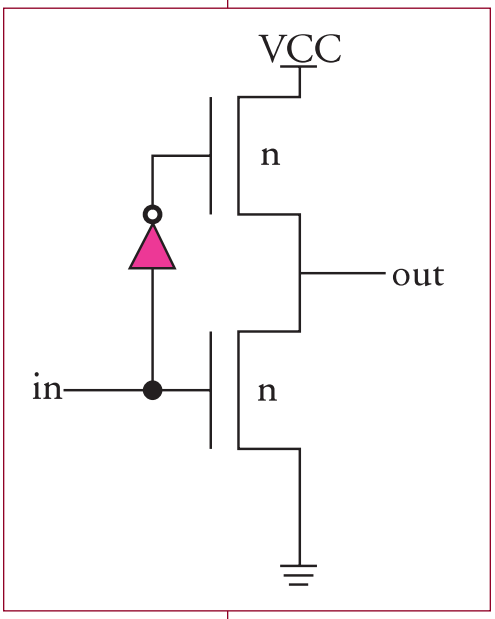


Figure 2.
Totem-Pole "TTL Output" Buffer

Continued on next page

CMOS I/O

Continued from previous page

Inputs

TTL input thresholds are compatible with older systems, and are popular in bus-oriented systems. TTL is therefore the default and the most popular input option. It means that a voltage below 1.2-V is interpreted as Low, while a voltage above 1.4-V is interpreted as High. This mimics the behavior of bipolar TTL circuits where this threshold is determined by two forward-biased silicon diodes. In Xilinx FPGAs, this "TTL" threshold is achieved by a reduced supply voltage on the input buffers, controlled by a global option that affects all device inputs.

CMOS inputs are specified such that a voltage below half the supply voltage is interpreted as Low, and a voltage above half of Vcc is interpreted as High. The actual threshold is usually somewhat lower than 50% of Vcc. In XC4000XL devices it is 38-40% of Vcc. For 5-V devices, the input threshold is globally selectable as either "TTL" or "CMOS"; the CMOS input option offers additional noise immunity and reduces static power consumption.

Inputs have a small amount of hysteresis, which makes the threshold for the rising edge a little higher than for the falling edge. Slow transitions will, therefore, switch cleanly, as long as there is no system noise greater than 100 mV. In a real system, this hysteresis does not make much difference. Slow transitions on data, control, and other combinatorial inputs just cause extra unpredictable delay. Slow transitions with more than 10 ns rise- or fall-time are very dangerous, since they invite any noise or ground-bounce to cause double triggering. ◆