Utilising FPGAs in Re-configurable Basestations And Software Radios

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Take a look at the circuit boards within any basestation and you will almost certainly find some sort of programmable device. Programmable logic was first used as glue logic replacement, but is now the preferred hardware solution chosen by many basestation designers.

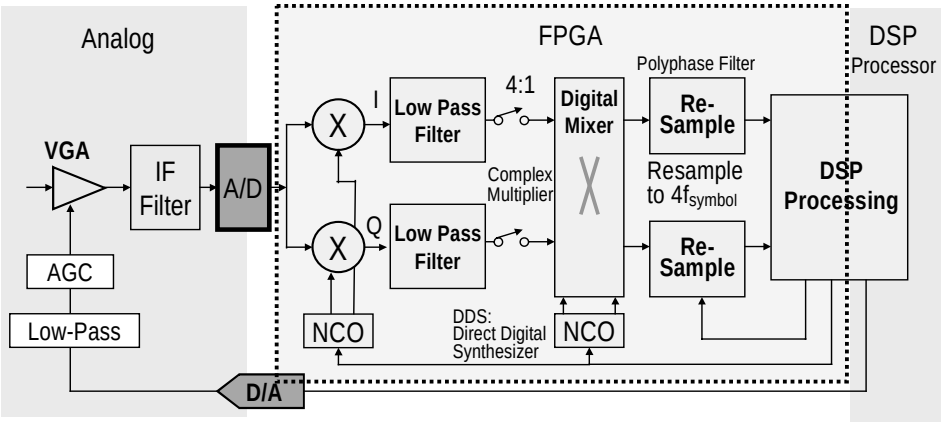
The digital components found in a basestation can be categorised into five main device types: Digital Signal Processors, Microprocessors/Microcontrollers, RAM, SRAM based FPGA programmable logic, Communication Chipsets (PCI, Ethernet, HDLC etc.). All but the last type can be completely reprogrammed in system.

It is therefore, now possible to produce a base-station in which the vast majority of its digital functionality can be changed remotely after it has been installed in the field. Not just the software code but the hardware as well. It allows the designer the opportunity to amend the functionality of the design all the way through the product life cycle. Changes may occur for a number of reasons including, rectifying design mistakes, a new system design requirement or adapting the system to meet evolving standards. It is the last point that fits in well with the way in which wireless systems have evolved.

When the architecture for GSM was first defined, it was not anticipated that it would be adapted to provide better data communications facilities. It is a testament to the systems architecture that such changes can be accommodated with the minimum of base-station redesign. Obviously much of this can be done in software because of the flexibility provided by Digital Signal Processors (DSP) and microprocessors. However, there are many parts of the system where DSPs and microprocessors cannot meet the performance required and this functionality has to be implemented in dedicated logic. Programmable logic allows the same degree of flexibility to hardware that software upgrades provide to the firmware.

FPGAs in Basestation Systems

FPGAs are particularly suited to the high speed filtering functions required after the analogue receiver, or for formatting the data prior to being sent to the transmit circuitry. For the receiver the data has to be filtered down to the baseband for suitable processing, usually by a combination of DSP and programmable logic. Typically, such filter functions are characterised as requiring a large number of simple Multiply and Accumulate (MAC) operations. The input data is also likely to be oversampled, typically by 4 or 8 times. This allows for digital filters to be designed with very steep roll-off characteristics. Figure 1 shows how the receiver part of such a system can be constructed.



FPGA Contribution

- Replace analog components: **>100 MHz data sample rates**
- FPGA for cycle intensive algorithms: **billions of MACs / sec**
- DSP processor for lower data rate, decision intensive algorithms

Figure 1: Block diagram of a possible receiver

A filtering operation is inherently a parallel operation, and the FPGA architecture is better suited to it than a sequential processing engine such as a standard DSP. DSP chips containing multiple DSP cores have been produced to try and improve the throughput. However, FPGAs can offer efficient solutions to problems that require hundreds of taps, and an equivalent MAC performance of several hundred of millions of MACs/sec.

Figure 2 shows various implementations of Root-Raised Cosine (RRC) Filters as defined in the UMTS radio interface specification (UTRA). The data width, over-sampling requirements, and number of filter taps vary from customer to customer, and are typically determined by the system designers.

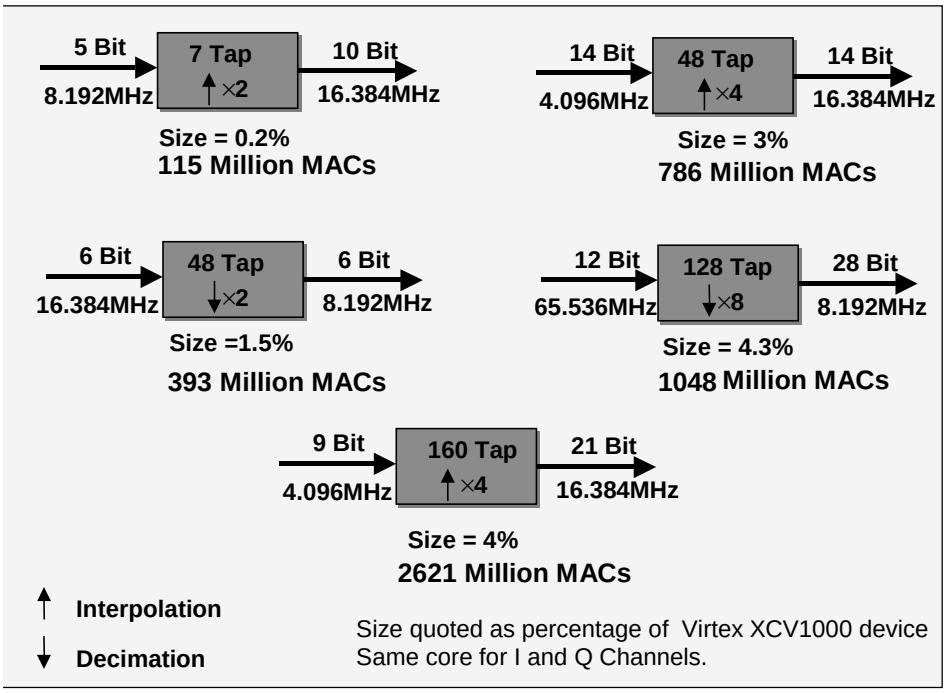


Figure 2: Examples of different UMTS Root Raised Cosine Receive and Transmit Filter specifications

Both the Transmit and Receive RRC filters can fit into relatively small FPGAs, or could become system modules within a larger FPGA if required. The filters operate in some cases at over 2000 Million MAC operations per second, although newer devices would be able to push this even higher if required. It is certainly possible to achieve Billions of MAC per second performance for a wide variety of filter designs.

The application of Xilinx FPGA devices in 3G W-CDMA systems

Xilinx is currently engaged with many base-station manufacturers to help develop their next generation of wireless communications systems. There is a great deal of uncertainty about many aspects of the next generation proposals, such as UMTS. There is also a requirement for demonstrator systems to be built for the NTT DoCoMo and UMTS programs. In order to meet the demanding timescales, engineers are implementing designs even while the specifications are changing. FPGAs have thus become a key enabling technology for these systems. They allow designers to begin board design and amend its functionality at all stages of the project, without having to re-layout and manufacture the printed circuit board.

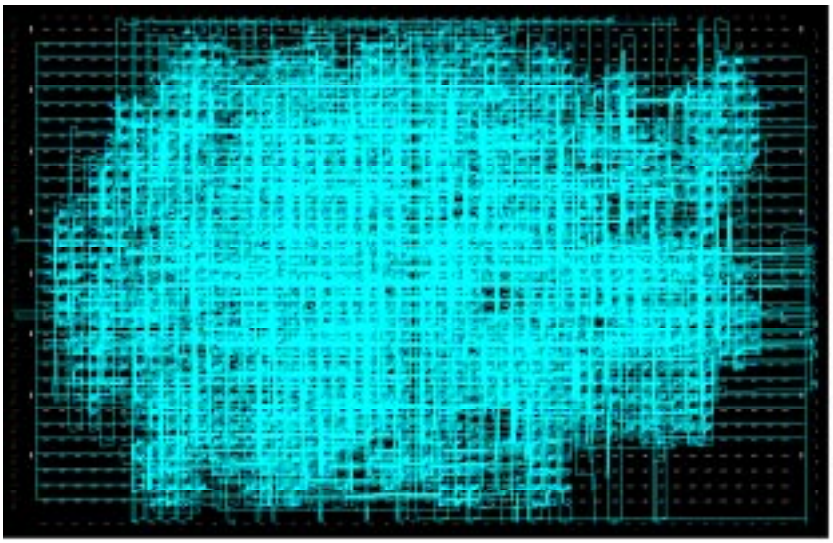


Figure 3: UMTS Matched Filter realised in 57% of a Xilinx Virtex XCV300 FPGA.

At the heart of the UMTS system lie the highly computationally intensive matched filters. Xilinx engineers have a UMTS Matched Filter design which operates on a 256 Chip correlation sequence, and can be reprogrammed to match any desired correlation sequence. The 8-bit two's complement input sample data is received at 4 times chip rate (16.384MHz) and processed to produce the 16-bit two's complement results with full precision. The design utilises 57% of a Xilinx Virtex XCV300 using the slowest speed grade, and achieves a processing rate of 1 GOPs. This is equivalent to 137K gates or only 14% utilisation of the largest Xilinx FPGA currently available – the Virtex XCV1000.

If the fastest speed grade is used, then utilising the same design implementation, it is possible to process at a rate of 8 MChip/sec. This provides a great deal of flexibility for future system enhancements.

Reprogramming the FPGAs in a basestation

Normally in a system as complex as a basestation, the FPGAs are configured under the control of a microprocessor or DSP. The configuration data is held in the system RAM and downloaded either to

each FPGA in turn via a serial chain or to each device at the same time in parallel. There are many other permutations, but essentially they are based around these two methods.

The microprocessor can receive data from either a local port, or via a control channel from the network. Data can be uploaded to the basestation, and depending on the operator's requirements can be scheduled for reprogramming immediately or at a later time. Most FPGAs currently available are always completely reprogrammed, this means that care has to be taken to ensure traffic is re-routed or disabled before reconfiguration takes place.

The latest Xilinx Virtex devices have the ability to be partially reconfigured. This allows designers in the future to reprogram only a part of the chip without disruption to other areas of the device. As programmable logic devices increase in size much more of the system functionality can be embedded within the device and partial reconfiguration will open up a lot more possibilities to system designers. Being able to reprogram specific functions within an FPGA will allow greater silicon efficiency, thereby reducing the size, power and cost of the FPGA required.

Development work is being undertaken to make both full chip and partial reconfiguration as simple as possible. Xilinx is spearheading this with a program called Internet Reconfigurable Logic (IRL). IRL simplifies the process of In-System Reconfiguration over any network by formalising the methods for doing so. The IRL initiative includes a suite of Java based enabling technologies to facilitate on board reprogramming. It covers the full spectrum of user requirements from very infrequent reprogramming for the purpose of field upgrades, to rapid, or run-time, reconfiguration of the programmable logic for applications that must change either data or logic on the fly.

Providing systems that can be reconfigured over any wired or wireless network provides the opportunity for a manufacturer to offer an operator an unprecedented level of flexibility in the deployment, maintenance and future proofing of a wireless network. This may seem far-fetched to some, however it is happening now in other networking technologies. Many of the routers at the heart of the World-Wide-Web IP Network, contain FPGAs whose code can be adapted either locally or remotely.

Jean Calvignac, IBM Fellow with IBM Corp. -- *"Our customers have been pleased to see product updates occur automatically via the network. These seamless updates have included both software and hardware changes. With its tools for Internet Reconfigurable Logic, Xilinx is broadening the appeal of this exciting technology."*

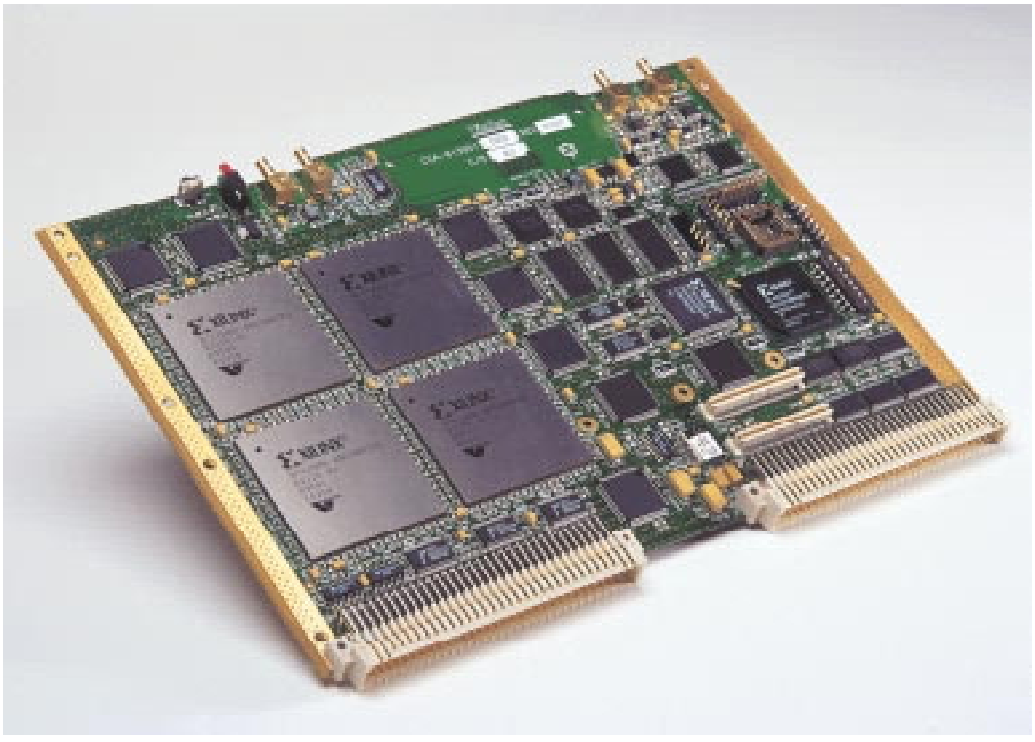


Figure 4: A re-programmable satellite modem.

High performance terminals & Software Radios

It is likely that FPGA technology will also be used to some extent in high-performance 3G wireless terminal equipment and Software Radios. Manufacturers have already deployed 2G and satellite mobile terminals that contain Xilinx FPGA devices. By exploiting deep-sub-micron process technology, FPGA devices are becoming much more power efficient. In conjunction with special power-down modes available on certain devices, they enable the low power stand-by and operational characteristics demanded by mobile terminals designers.

Summary

The use of FPGA technology in combination with other programmable technologies such as DSP and Microprocessors has enabled wireless basestation manufacturers to offer an unprecedented level of service and flexibility to their products.

The Third generation wireless networks will be able to exploit this technology even further. The likelyhood of having to support multiple air interface standards, and the very aggressive rollout plans for such networks, ensure that FPGA devices will become increasingly key components in such systems. The ability to change configuration when in the field ensures an extra degree of flexibility for the manufacturers and network operators.