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HDL VERIFICATION SPECIAL SECTION

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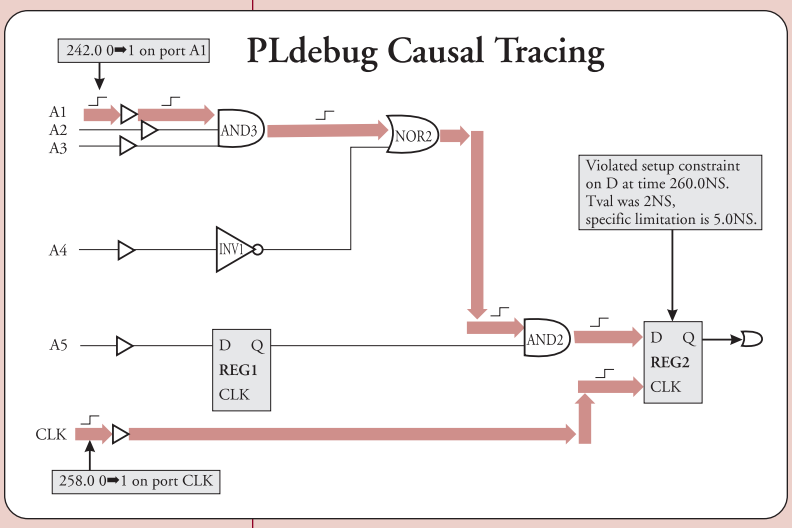
Using Synopsys SmartModel FPGA

FPGAs are often the most critical part of a system and must be extensively tested. However, today's designs are typically too large and too complex to rely on manual debugging methods; strong verification and debugging tools are required.

SmartModel FPGA models, known as SmartCircuit, provide you with the advanced verification and debugging features that are required to successfully verify your design in the shortest timeframe. The SmartCircuit models are basically templates of unconfigured devices. The models are programmed by a design netlist in the same format produced by the Xilinx place and route tools (standard EDIF). The SmartCircuit FPGA increases productivity by allowing you to focus on the design and system verification tasks rather than the simulation details.



PLdebug - Advanced Debugging and Event Tracing

One key to successfully verifying a design is the ability to quickly debug functional and timing errors. The SmartCircuit PLdebug feature allows you to do just that, by causally tracing back to the root cause of any logic event or timing error. Without PLdebug you would be forced to manually analyze hundreds of possible paths to identify a logic or timing error.

If you encounter functional or timing errors during a simulation run, it is imperative to trace them back to the parent event that is the root cause. In a large design this is usually a very complex task. The PLdebug feature uses an automated history mechanism to deliver this capability while making a minimal performance effect on the simulation. The causal tracing features work from user-specified trigger points to perform the following tasks:

- Trace back to locate the root cause of any logic event error.
- Trace forward to find the effects of any specific logic event.
- Identify the root cause of any timing constraint violation.

The PLdebug reports quickly identify the root of the logic or timing error by generating a list of events internal to the FPGA that are causally related to the problem event.

FIGURE 1 - CAUSAL TRACE

```
SmartModel TRACE:

Instance /TESTBENCH/DUT/
  SMART(XC4005E_84),at time 586.3 NS.

Beginning cause report from "DBUS<6>":

586.3 ns Z->X on model port DBUS<6>

586.3 ns Z->X on cell port /XSYM4/O,
  net DBUS<6>

586.3 ns 1->0 on cell port /XSYM4/T,
  net DBUS_ENABLE<0>

569.4 ns 1->0 on cell port /XSYM40/
  O,net DBUS_ENABLE<0>

564.9 ns 0->1 on cell port /XSYM44/O,
  net ENABLEBUS_SIG

562.6 ns 1->0 on cell port /XSYM43/O,
  net U2;N735

560.6 ns 0->1 on cell port /XSYM42/O,
  net YSIG2

558.1 ns 0->1 on cell port /U2;MODE<1>/
  Q,net U2;MODE<1>

555.3 ns 0->1 on cell port /U2;MODE<1>/
  C,net CLOCK1

553.9 ns 0->1 on cell port /BUFGS_TL/O,
  net CLOCK1

550.0 ns 0->1 on model port CLOCK

Report completed.
```

Note: The report is triggered on a user-specified event and then traces that event back through time to the parent event. In this case the parent event is the CLOCK port.

Adapted from a Synopsys Application Note.

Models to Verify Xilinx FPGA Designs

FIGURE 2 - EFFECT TRACE

```
SmartModel TRACE:

Instance /TESTBENCH/DUT/
  SMART(XC4005E_84),at time 1087.1 NS.

Triggering effect report from “DBUS<6>”
  at 1087.1 ns:

1087.1 ns Effect 0->X on cell port /
  XSYM3/O,net U3;N163

1090.9 ns Effect 0->X on cell port /
  XSYM50/O, net YSIG6

1090.9 ns Effect 0->X on cell port /
  U3;I<6>/D,net YSIG6

Report completed.
```

By tracing the effect of an 0 to X transition on the DBUS<6> port *(see **Figure 2**)*, you can see that the X propagates through the design to the U3/I<6> instance net. You can control the scope of the report, and target multiple events and simulation times.

FIGURE 3 - CAUSAL TRACE TRIGGERED BY TIMING CONSTRAINT VIOLATION

```
SmartModel ERROR:

Violated pulsewidth constraint PW_CLR+
  on CLR for cell U2;MODE<1> at time
  12.1 ns.


Actual pulsewidth time 3.0ns, specified
  minimum is 4.0 ns.

Instance /TESTBENCH/DUT/
  SMART(XC4005E_84),at time 12.1 NS.


SmartModel TRACE:

Constraint causal report for event on
  “CLR” at 12.1 ns:

12.1 ns 1->0 on cell port /XSYM72/O,
  net YSIG27

10.5 ns 1->0 on cell port /XSYM37/O,
  net U2;N658

5.5 ns 0->1 on cell port /XSYM33/O, net
  N4

3.0 ns 0->1 on model port RESET

Report completed.
```

Using Pldebug you can quickly identify the source of a functional error and the source of a timing constraint violation. In **Figure 3**, you can see that the source of the timing violation was a short pulse on the RESET port.

Advanced Debugging - Windows and Monitors

Visibility into the FPGA design during simulation is another critical success factor. The ability to trace the contents of an internal net or register will aid in the debugging of the overall design. Another feature of the SmartCircuit FPGA models is the ability to look inside the FPGA design using the Windows feature — no longer is the FPGA a black box within the simulation. The Windows feature allows you to trace, in the simulation waveform window, any nets, ports, or states. This gives you full visibility into the design at a level that is easily understood. Having this visibility substantially eases the FPGA verification process and the subsequent debugging. You can trace the designated nets, ports, or states and force values on them, allowing you to recreate corner cases and evaluate a design's functionality in those cases. The monitor feature enables you to create a text print-out of the values on the nets, ports, or states in the selected portions of the design within the simulator's transcript window.

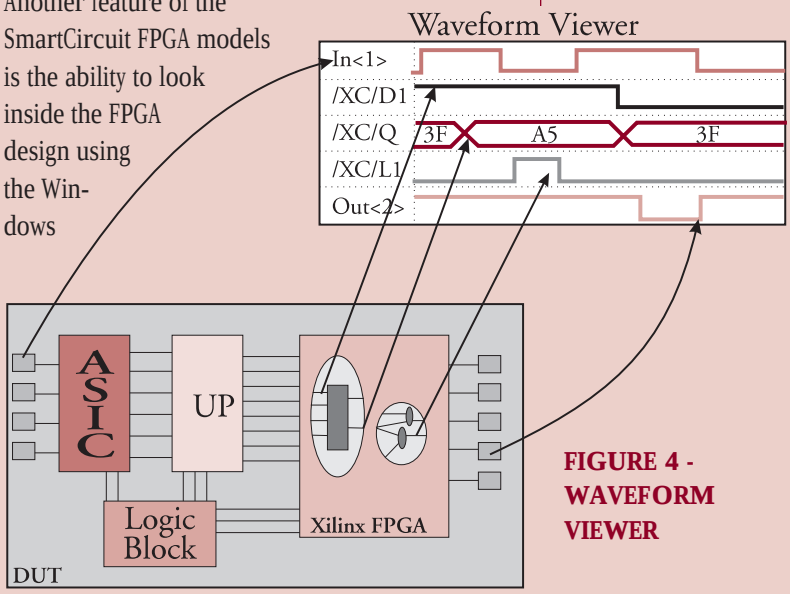


FIGURE 4 - WAVEFORM VIEWER

Advanced Debugging - Visual SmartBrowser

Visual SmartBrowser (VSB) allows you to visually display the FPGA netlist using an on-demand viewing technique. With very large and complex FPGA designs, you are typically only interested in a small section of the netlist. VSB allows you to

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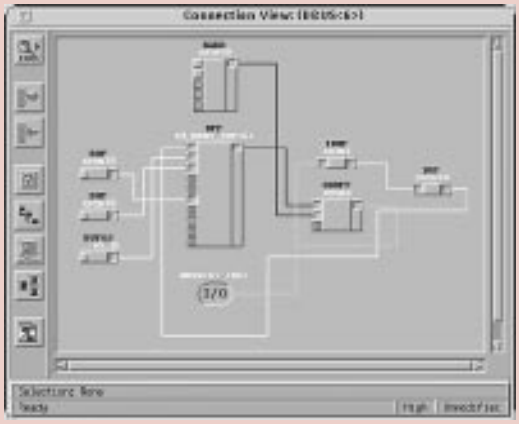

FIGURE 5 - VISUAL SMARTBROWSER

concentrate on only the section that interests you.

VSB also incorporates a set of tools that allow you to identify sections of the design you want to display. VSB then generates the model command file (mcf) required to make these sections available in the simulation. The only file that you have to create, to simulate using a SmartCircuit model, can be automatically generated using VSB.

Advanced Debugging - VSB helps identify where a timing constraint fix should be implemented

VSB is run on the SmartCircuit netlist that contains all of the design's specific delay and timing information, extracted from the original vendor netlist. This delay and timing information is put at your fingertips using the VSB examine cell view**.**

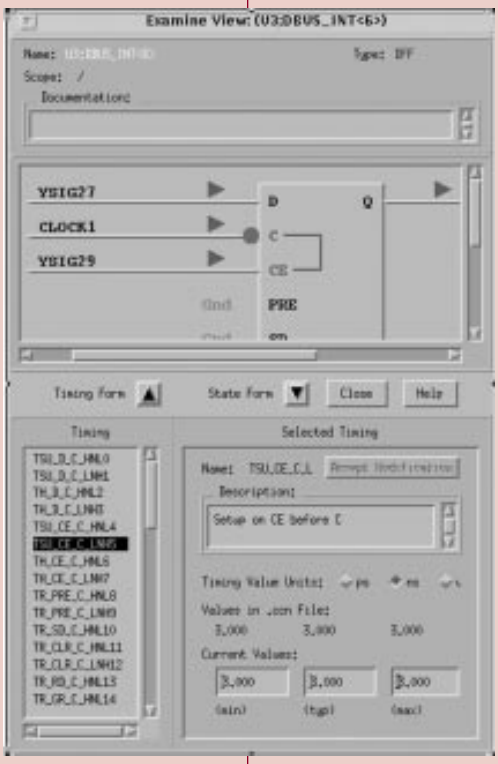

FIGURE 6 – EXAMINE CELL VIEW

After using PLdebug to identify the root cause of a timing violation you can view the actual delays being used by each cell in that specific path. You can then use VSB to change the timing of any parameter on the cell and thus experiment with "what if" scenarios. The incremental changes do not affect the source netlist, but allow you to exactly identify where the problem lies. With that information you can return to the original source of the design and fix the problem. Doing very quick incremental changes on the SmartCircuit netlist, to evaluate if a change does fix the problem, speeds up the overall design cycle.

SmartModel FPGA models fit straight into your existing design flow.

Below is a simplified view of the design flow using SmartModels in system verification.

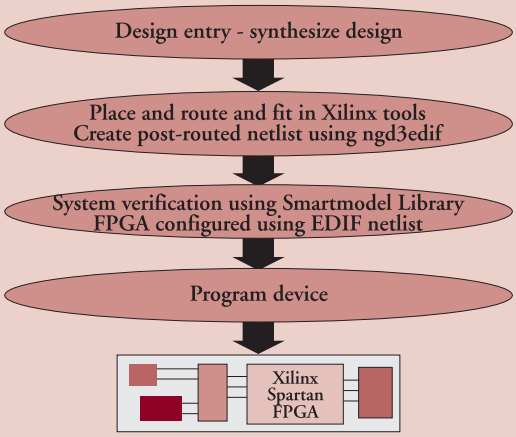

FIGURE 7 – SMARTMODEL DESIGN FLOW

Using SmartModels with Xilinx Alliance Tools

You don't need to do anything special in the Xilinx Alliance Series tools to target a SmartCircuit FPGA model. The following options must be selected in the Design Manager tool:

- From the design pull down select **implement and options**. Select **edit implementation template**. In the **Interface** section make sure that the simulation data options are set to **Generic EDIF**. (These are the Design Manager Tools default settings.)
- Under **implement options** make sure **Produce Timing Simulation Data** is selected under the **Optional Targets** section. (Configuration Data is checked by default.)
- Run the tools as normal and they will produce a time_sim.edn file. This is your post-routed netlist file that will be used to configure the SmartCircuit models.

Conclusion

Using SmartModel FPGA models from Synopsys can save valuable time and minimize the difficulty of verifying and debugging complex FPGA designs

For full SmartModel documentation see the Synopsys home page at, http://www.synopsys.com/products/lm/docs/swift_r41/intro.html. ◆