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HDL VERIFICATION SPECIAL SECTION

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Viewlogic's Mixed-Design Verification Methodology

Viewlogic Systems offers a comprehensive and flexible environment for language-based design using VHDL or Verilog, or a combination of both. By supporting multiple design styles and by allowing styles to be mixed, Viewlogic has created a verification flow that is flexible enough to encompass a wide range of design methodologies. You have the ability to verify functionality prior to synthesis, after synthesis, and after place and route from the Fusion simulation environment. With tight integration to board-level design, verification can even be extended to systems with multiple FPGAs.

Design Entry Options

The benefits of using hardware description languages (HDLs), such as VHDL or Verilog, are numerous, especially when you consider the ever increasing device densities such as those available in the Xilinx Virtex family. Language-based design provides you with the ability to work at higher levels of abstraction, increasing productivity and reducing design costs.

A significant advantage of language is that it enables functional verification prior to committing a design to a particular technology. Once functional correctness has been verified, the design can be input to a language synthesis tool, such as FPGA Express, for optimization to the selected Xilinx device family.

At Viewlogic, we have found that language is not well suited to all types of design description. Some designers prefer using a block diagram for their top-level structural instantiation as opposed to writing structural VHDL or Verilog; some system houses require schematics at the top.

In other cases, designers may find it easier to use bubble diagram graphical editors for state machine entry. Being able to mix and match these alternative design styles and verify them in a single process is critical to design success. The use of IP cores may also require you to instantiate language modules into a block diagram, thereby requiring a verification environment that can handle a mix of design styles.

Co-Simulation with the Fusion Verification Environment

To handle this complete variety of mixed design styles, Viewlogic offers the Fusion simulation environment. Fusion is an environment that encompasses four simulators. There are three digital simulators and one analog simulator. The digital simulators are:

- Fusion/ViewSim for gate level simulation.
- Fusion/Speedwave for VHDL.
- Fusion/VCSi for Verilog simulation.

In the Fusion environment, you can use any one of the simulators, or a mix of all three. Each simulator operates on its piece of the design, fully communicating with the other simulators as the design dictates. You see the output presented as if the Fusion environment were a single simulator; there is one set of input stimuli and one set of output.

Functional Verification

Before committing your design to place and route or synthesis, you should verify that your design is functionally correct; finding bugs early in the design cycle makes them much easier to resolve. Viewlogic gives multiple options for functionally verifying your design.

For pure schematic designs, after schematic capture you perform gate-level simulation in the Viewlogic Fusion/ViewSim simulator. Xilinx provides a complete set of ViewSim models with the Alliance Series software that enables you to simulate these schematics. You can translate your schematics into a ViewSim netlist, load the design into ViewSim, stimulate your design, and verify the results. Stimulus is provided via the ViewSim command language. Usually, these commands are executed from a file, but they can also be run interactively. ViewSim has the ability to check outputs against a given set of inputs, which gives it

a regression capability, and ViewSim can also generate a waveform file, which can be inspected in the Vwaves waveform reader program.

VHDL designs can be verified with the Fusion/SpeedWave VHDL simulator, and you will usually write a testbench to stimulate and verify your designs.

If you are using Verilog, your design can be verified with the Fusion/VCSi Verilog simulator. Like SpeedWave and ViewSim, Fusion/VCSi is accessed from the Fusion simulation environment. Now you have the option of using a ViewSim command file or a Verilog test fixture. The test fixture and Verilog design files are loaded into Fusion/VCSi where they are compiled on the fly and automatically loaded into the Verilog simulator. Again, like SpeedWave and ViewSim you can generate waveform files for inspection in Vwaves.

An additional advantage of Verilog is the PLI programming language interface. The PLI defines how to interface user-defined C language functions with a Verilog design. This means that you can co-simulate your Verilog design with the C functions.

Viewlogic's Fusion simulation environment also supports mixed design styles such as a top-level schematic with underlying VHDL and/or Verilog blocks for representing state machines or synthesizable cores. Through Viewlogic's Fusion environment, you have the ability to functionally simulate schematics containing Xilinx primitives with VHDL blocks and Verilog blocks. The power of this environment is that you keep your full language debugging capability seamlessly flowing among gate-level, VHDL, and Verilog simulation. When you use this methodology, you will typically write your stimulus in ViewSim command format and not use HDL testbenches or test fixtures

Post-Synthesis Simulation

Post-synthesis simulation is used to verify that your VHDL or Verilog code was synthesized into the logic you expected. FPGA Express has the ability to output VHDL and Verilog netlists representing the synthesized design. It is at this point that your testbench or test fixture can be used again. This time the unit under test is not your original code but is the top-level entity/module of the netlist synthesized by FPGA Express. The synthesized netlist is written as structural VHDL or Verilog, instantiating primitives from the Xilinx UNISIM library with the primitive behaviors defined. By using this netlist in conjunction with the UNISIM library and your testbench/test fixture, your design can be verified. Note that FPGA Express can also output these netlists with the primitive behavior defined.

Post Place-and-Route Simulation

After place and route, the Xilinx Alliance Series tools can output a structural netlist in Viewlogic-compatible EDIF, VHDL, or Verilog. If you are creating schematic-based designs, you will most likely choose EDIF. This timing-embedded EDIF can be converted into a ViewSim netlist, which can be very useful if you are also using ViewSim for board level verification. If you choose this path, you can use your original simulation command file to verify timing through your design. If you are doing VHDL or Verilog designs, you may also choose EDIF or you can have the Alliance Series Core tools output structural VHDL or Verilog with a corresponding SDF timing file instead. Unlike the structural netlist generated by FPGA Express, the structural VHDL and Verilog netlists output by the Xilinx Alliance Series tools instantiate SIMPRIM primitives. Xilinx provides libraries for the SIMPRIM primitives for use with Fusion/ViewSim, Fusion/SpeedWave (VHDL/VITAL), and Fusion/VCSi (Verilog).

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Conclusion

As you move from schematics to language-based design, it is important to have an environment that allows multiple verification options. Viewlogic provides a set of tools for language verification, schematic verification, and mixed schematic/language-based verification. Xilinx, through its UNISIM and SIMPRIM libraries, provides the models that enable these flows. By covering these three types of design styles, you may pick a verification flow that best suits your design methodology.

For more information on the Viewlogic solution for FPGAs and other types of programmable devices, contact Viewlogic at 1-800-873-8439 or visit our website at www.viewlogic.com ◆