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### Features

- Data widths from 2 to 32 bits
- Drop-in modules for the XC4000E, EX, XL, XV and Spartan families
- High performance and density guaranteed through Relational Placed Macro (RPM) mapping and placement technology
- Available in Xilinx CORE Generator

### Functional Description

This macro is a four-input multiplexer. One input is chosen by the state of the Select lines (S0 and S1) and directed to the output bus.

### Pinout

Port names for the schematic symbol are shown in Figure 1 and described in Table 1.

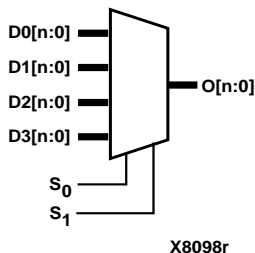


Figure 1: Functional Representation

Table 1: Core Signal Pinout

Signal	Signal Direction	Description
D0[n:0]	Input	FIRST INPUT - selected when S0 = 0, S1 = 0
D1[n:0]	Input	SECOND INPUT - Selected when S0 = 1, S1 = 0
D2[n:0]	Input	THIRD INPUT - Selected when S0 = 0, S1 = 1
D3[n:0]	Input	FOURTH INPUT - Selected when S0 = 1, S1 = 1
S0, S1	Input	SELECT INPUT - chooses which input data bus is directed to the output bus.
O[n:0]	Output	OUTPUT BUS

### CORE Generator Parameters

The CORE Generator parameterization window for this macro is shown in Figure 2. The parameters are as follows:

- **Component Name:** Enter a name for the output files generated for this module.
- **Port Width:** Select a bit width from the pull-down menu. The valid range is 2-32.
- **Create RPM:** When checked, a columnar Relational Placed Macro is created.

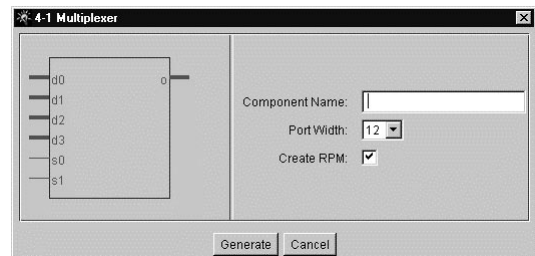


Figure 2: Parameterization Window

## Core Resource Utilization

Table 2 shows the number of CLBs required for each available bit width.

**Table 2: Bit Width versus CLB Count**

Bit Width	CLB Count
2	2
3	3
4	4
5	5
6	6
7	7
8	8
9	9
10	10
11	11
12	12
13	13
14	14
15	15
16	16
17	17
18	18
19	19
20	20
21	21
22	22
23	23
24	24
25	25
26	26
27	27
28	28
29	29
30	30
31	31
32	32

## Ordering Information

This macro comes free with the Xilinx CORE Generator. For additional information contact your local Xilinx sales representative, or e-mail requests to [coregen@xilinx.com](mailto:coregen@xilinx.com).

### Parameter File Information

Parameter Name	Type	Notes
Component_Name	String	
Port_Width	Integer	2 - 32
Create_RPM	Boolean	True/False