ALLIANCE
Series Software

XILINX®

Exemplar
Implementation Flow

Module Generators

LogiBLOX

CORE Generator

.NGC= Xilinx Binary Netlist

.V
.VHD

.NGC

.VEI
.VHI

.VEO
.VHO

Verilog & VHDL Instantiation

Renoir

Schematic Design Editor

HDL Editor

VHDL Verilog

VHDL Verilog

VHDL Verilog

XNF *
EDIF

VHDL Verilog

Timing Requirements

.EDN

Functional Simulation Flow

CORE Generator

LogiBLOX

UNIFIED

Gates

UniSim

VITAL & Verilog

SimPrim

VITAL, Verilog, & Gates

HDL Test Bench

Command File or Test Vectors

3rd Party

S I M U L A T I O N

VHDL Verilog

SDF

Timing Simulation Flow

EDIF

BIT JEDEC

STAMP Model

Reports

Xilinx

I M P L E M E N T A T I O N

Tools

(X) exemplar

LEONARDO SPECTRUM

EG

NCF

Design Constraints

XNF EDIF

VHDL Verilog

EDIF Netlist

User Constraints File

.VHD
.V

EDDIE g 1999

PN 0010420 01

Functional Simulation Flow

Note:
* XNF primitives only. Timing information is not passed from schematic.

Exemplar
Information

Device Architecture Support

FPGA Product Family
Spartan
Virtex
XC4000X

CPLD Product Family
XC9500

Recommended Settings

For recommended settings, go to
http://www.xilinx.com
"Product" → "Software Solutions"

Xilinx
Contacts and Technical Support

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1-503-685-7750
Hoa Dina, Technical Support Manager
1-510-337-3700

HDL Library and Language Support

HDL Libraries meet all the HDL Standards
IEEE 1076, -87, & -93, IEEE 1164 VHDL OVI 2.0
and Verilog-XL
Libraries include: • **std_logic_1164**
• **std_logic_arith** • **std_logic_signed**
• **std_logic_unsigned** • **attributes**

Guide Overview

1
Invoke Leonardo Spectrum

Invoke the Leonardo Spectrum synthesis tool
When the dialog box appears, select
Leonardo Spectrum Level X as appropriate.

2
Synthesis Wizard for New Users

When the tool first invokes, a **synthesis wizard**
will appear. The wizard provides a step-by-step
guide through the synthesis process for new
users.

3
Tab-based GUI for Advanced Users

For advanced users, cancel wizard. The full
featured **tab-based GUI** of Leonardo Spectrum
Level X window will appear.
There are two ways of using tab-based GUI:
Use **Quick Setup** or use **individual tabs until**
output which provide more control and options.

4
Specify Input Files

To instantiate any Xilinx component,
Click right mouse button to **Set Technology All**
on input file.

5
Select Target Architecture

Select Target device and speed grade.

6
Synthesis Commands

Use individual tabs to set up options and
constraints with more control. Please refer to
the online documentation for information on
how to specify options and constraints.

7
Synthesize

Push **Run Flow** button to synthesize.