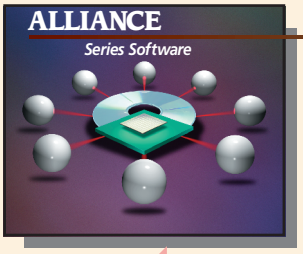

Synopsys FPGA Compiler Implementation Flow

Module Generators

3rd Party Schematic Simulator

May require user defined symbol if not part of a Xilinx provided interface.

EDN

LogiBLOX

CORE Generator

.V .VHD

.NGC= Xilinx Binary Netlist

NGC

.VEI .VHI

VEO VHO

Verilog & VHDL Instantiation

State Diagram Editor

Schematic Design Editor

HDL Editor

VHDL Verilog

VHDL Verilog

XNF EDIF

VHDL Verilog

EDN

Black Box Instantiation

Synthesis & DesignWare Libraries

Functional Simulation Flow

Timing Requirements

CORE Generator

LogiBLOX

UNIFIED

Gates

UniSim

VITAL & Verilog

SimPrim

VITAL, Verilog, Gates

HDL Test Bench

Command File or Test Vectors

VSS VCS or 3rd Party SIMULATION

Timing Simulation Flow

VHDL Verilog

SDF

EDIF

BIT JEDEC

Reports

Xilinx IMPLEMENTATION Tools

SYNOPSYS FPGA Compiler

DC2NCF

NCF

SXNF SEDIF

VHDL Verilog

Timing Constraints

Synopsys XNF and Synopsys EDIF (SEDIF for Virtex and Spartan II)

User Constraints File

Functional Simulation Flow

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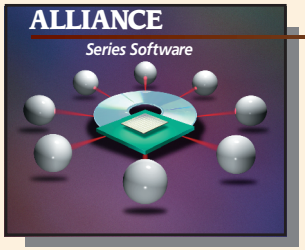

Synopsys FPGA Compiler Information

Device Architecture Support

FPGA Product Family
Spartan
Virtex
XC4000X

CPLD Product Family
XC9500

Recommended Settings

Please refer to your A2.1i software installation and the example:
template.synopsys_dc.setup_fc
.synopsys_vss.setup
and the runscript files in
$XILINX/synopsys/examples

Xilinx Contacts and Technical Support

World Wide Web:
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33 1-3463-0100
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Synopsys Contacts and Technical Support

World Wide Web:
http://www.synopsys.com
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1-800-245-8005
support_center@synopsys.com

Guide Overview

1 Setup FPGA Compiler .synopsys_dc.setup file

Use the **template.synopsys_dc.setup_fc** examples in the **$XILINX/synopsys/examples**. Add the correct information for your target die and speed grade. Modify the paths for your setup.

2 Create a compile script to read your input files

Use the example compile scripts in the **$XILINX/synopsys/examples** as a guide. Create a compile script to read all the HDL files for the design.

3 Synthesize the design by running the compile script with dc_shell or design_analyzer

Compile the design by running:
dc_shell -f runscript |tee run.log
or
design analyzer &
Either step will produce a .sxnf file

4 Place and Route the .sxnf or .sedif * file using the A2.1i software

Place and route the synthesized design via the **UNIX A2.1i commands**
or the
Design Manager GUI.

*** .sedif for Virtex and Spartan II**

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