GVA-270 Virtex™-E DSP Hardware Accelerator

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Features

- 65 MHz maximum input A/D sample rate
- 30 MHz sample Bandwidth
- Each FPGA has a dedicated A/D
- Each FPGA has access to both A/Ds and D/As (via local bus)
- FPGA Logic Expansion (50K to over 1.5M gates per FPGA)
- Each FPGA has a Dedicated 256K x 18 ZBT SRAM
- Up to 393,216 bits of internal Block RAM
- Eight Delay Locked Loops (DLL)
- On Board DLL clock synchronization between FPGAs
- External DLL clock synchronization for multi-board configuration.
- 78-bit FPGA Local Bus with External Data Access
- Slave Serial and Download Cable (Model DLC4 with 3 V adaptor) Configurable
- 60 MHz maximum output D/A sample rate
- Separate FPGA Power Plane for Power Measurement
- External 1.8V Jack for High Current FPGAs
- Programmable A/D Sample Clock
- On Board 60 MHz Clock Oscillator
- External High Stability Clock Input

General Description

The GVA-270 Digital Signal Processing Hardware Accelerator is designed for the implementation of complex DSP or other channel coding designs. This platform provides a highly flexible environment for the integration of various software and hardware DSP applications using the Xilinx Virtex™-E FPGA family.

The GVA-270 supports the following Xilinx Virtex-E FPGAs:

- XCV50E-4PQ240C
- XCV100E-4PQ240C
- XCV200E-4PQ240C
- XCV300E-4PQ240C
- XCV400E-4HQ240C
- XCV600E-4HQ240C
- XCV1000E-4HQ240C

Functional Description

The platform's general configuration consists of an I and Q channel which is passed through a 12th order low pass filter. The 12th order low pass filter band limits the input signals to a 30 MHz bandwidth. The signal rejection is -58 dB at 40 MHz. Next, the signals are digitized by a 12 bit A/D. The sample rate (maximum of 65 MHz) of the A/D is programmable since it is generated by the Xilinx FPGA. The digitized signals are now ready to be processed by the customer's algorithm that is implemented in hardware by either of the two Xilinx FPGAs. Once the signals have been processed, a 120 MSPS D/A via the XILINX FPGA can convert them back to an analog waveform. The processed data may also be sent to the external data port. The processed analog waveforms are passed through a 12th order smoothing filter which is band limited to 30 MHz. The filtered analog signal is connected to a 50 ohm SMA output for viewing

Each Xilinx FPGA has access to an external 256K x 18 bit ZBT SRAM that could be used for temporary data storage. Each Xilinx FPGA supported, has 65536 to 393,216 bits of internal Block RAM.

The I-channel Xilinx FPGA may also access unused address space in the configuration Flash EPROM by interfacing to the CPLD via the local bus. The two Xilinx FPGAs have a 78 bit local bus that allows for the direct transfer of data between the two devices and other external devices. Using the 78 bit local bus, the I and Q channel FPGAs could be configured to have an off-board interface to an external processor such as a TMS320C31 or other Digital Signal Processor. For non-specific clock requirements, an external clock source is available. Each Xilinx FPGA has eight Delay Locked Loops (DLL) for system clock synchronization. An external DLL clock and connector has also been provided to allow the synchronization of two GVA-270 Hardware Accelerators or between the two on-board FPGAs.

Ordering Information

This product is available directly from GV & Associates. Please contact them for pricing and more information.

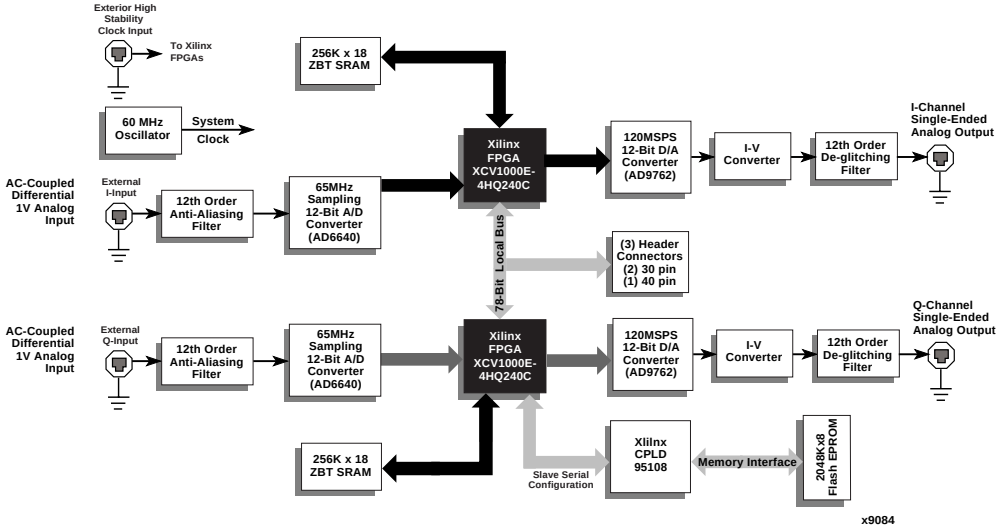

Figure 2: GVA-270 Virtex FPGA Block Diagram

Related Information

Xilinx Programmable Logic

For information on Xilinx programmable logic or development system software, contact your local Xilinx sales office, or:

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