CAST, Inc.

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Features

- Programmable data word length, parity and stop bits
- Parity, overrun and framing error checking instructions and counting loop interactions
- Supports transmission rates over the 1.0 Mbps spec
- False start bit deletion
- Peripheral modem control functions
- Functionality based on the Motorola MC6850

Applications

The C6850 core is used in serial data communications and modem applications.

AllianceCORE™ Facts

Core Specifics	
See Table 1	
Provided with Core	
Documentation	Core documentation
Design File Formats	.ngo, .XNF Netlist; VHDL Source RTL available extra
Constraint Files	.ncf
Verification Tool	VHDL
Schematic Symbols	Viewlogic
Evaluation Model	None
Reference designs & application notes	None
Additional Items	None
Design Tool Requirements	
Xilinx Core Tools	Alliance/Foundation 1.5
Entry/Verification Tool	VHDL RTL
Support	
Support provided by CAST, Inc.	

Table 1: Core Implementation Data

CPLD	Macrocells[2]	Product Terms[2]	I/O[1]	Performance[2] (MHz)	Speed Grade
XC9500	118	556	29	TX: 40.8 RX: 71.4	-7
XC9500XL	118	532	29	TX: 96.1 RX: 158.7	-5

FPGA	CLBs	Global IOBs	IOBs[1]	Performance (MHz)	Speed Grade
XC4000XL	86	4	25	52.2	-09
Spartan	86	4	25	54.0	-4

Notes:
1. Assuming all core I/O are routed off-chip.
2. CPLD figures stated are for speed-optimized place and route run through version 1.5 of Xilinx tools.
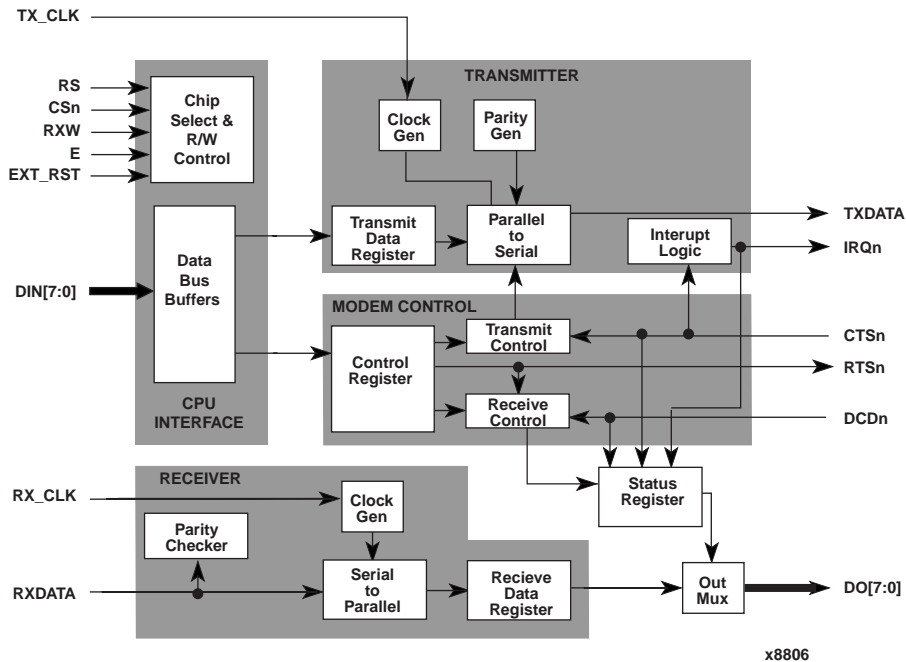
Figure 1:   C6850 Block Diagram

General Description

The C6850 asynchronous communications interface (ACIA) core provides data formatting and control to the asynchronous data communications of data bus systems.

The core has select, enable, read/write, interrupt and bus interface logic features that allow data transfers over an 8-bit bi-directional parallel data bus system. With proper formatting and error checking, the core can transmit and receive serial data.

 In addition, a programmable control register provides the core with a transmit control, a receive control, an interrupt control, variable word lengths and clock division ratios. Three control lines are provided for peripheral or modem operation

Functional Description

The C6850 core is partitioned into modules as shown in Figure 1 and described below.

Modem Control

The Modem Control Logic consists of a set of signals that can be used to interface with almost any modem. These standard signals consist of CTSn, RTSn and DCDn. The Transmit and Receive Control Blocks and Control Register Block monitor and control these signals.

Receiver

The Receiver section accepts serial data and converts to parallel format. It also checks for parity, framing, overrun, and break and then sends the formatted data to the CPU. The Receiver section is made up of the Parity Checker, Clock Generator, Serial to Parallel and the Receive Data Register.

Transmitter

The Transmitter section accepts parallel data from the Data Bus Buffer, converts it to serial inserting all required bits depending on the communication protocol and outputs the formatted serial stream to the TxData output pin. The Transmitter section is made up of the Transmit Data Register, Transmit Control, Clock Generator, Parity Generator, Parallel to Serial and Interrupt Logic Blocks.

Status Register

Information on status of C6850 is available to CPU by reading the status register (read only register).

Output MUX

The Output MUX selects between the Status register and the data register.

CPU Interface

The CPU Interface receives control signals from the CPU. These signals consist of the data bus read and write signals, chip selects, reset and master clock signals. The Data Bus Buffer Block is used by the CPU to write data to the device using the above signals.

Core Modifications

The C6850 core can be customized to include a 16 bit Internal Baud Rate Generator. Features which are not required can be removed to improve the efficiency of the layout.

Please contact CAST directly for any required modifications.

Pinout

The pinout of the C6850 core has not been fixed to specific FPGA I/O, allowing flexibility with a user's application. Signal names are shown in the block diagram in Figure 1 and in Table 2.

Verification Methods

The C6850 core's functionality was verified by means of a proprietary hardware modeler. The same stimulus was applied to a hardware model which contained the original Motorola chip, and the results compared with the core's simulation outputs.

Recommended Design Experience

The user must be familiar with HDL design methodology as well as instantiation of Xilinx netlists in a hierarchical design environment.

Ordering Information

The C6850 core is available from CAST, Inc. The C6850 core is licensed from Moxsyn S.r.l. Please contact CAST, Inc. directly for pricing and information.

Related Information

Microprocessor, Microcontroller and Peripheral Data Book (Vol. II),1988

Contact:
Motorola Inc.
Literature Distribution Center
6501 William Cannon Drive West
Austin, Texas 78735-8598
URL: http://motorola.com

Table 2: Core Signal Pinout

Signal	Signal Direction	Description
TX_CLK	Input	Transmit clock; uses 1 global IOB pin
RS	Input	Register Select
CSn	Input	Chip Select
RXW	Input	Read /Write
E	Input	Enable (clock); uses 1 global IOB pin
EXT_RST	Input	External reset
DIN[7:0]	Input	Data Input Bus
RX_CLK	Input	Receive clock; uses 1 global IOB pin
RXDATA	Input	Receive Data
TXDATA	Output	Transmit Data
IRQn	Output	Interrupt Request
CTSn	Input	Clear-to-Send
RTSn	Output	Request-to-Send
DCDn	Input	Data Carrier Detect; uses 1 global IOB pin
D0[7:0]	Output	Data Output Bus

Xilinx Programmable Logic

For information on Xilinx programmable logic or development system software, contact your local Xilinx sales office, or:

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