C8255A Peripheral Interface

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Features

- Three 8-bit Peripheral Ports - Ports A, B, and C
- Three programming modes for Peripheral Ports: Mode 0 (Basic Input/Output), Mode 1 (Strobed Input/Output), and Mode 2 (Bidirectional)
- Total of 24 programmable I/O lines
- 8-bit bidirectional system data bus with standard microprocessor interface controls
- Functionally based on the Intel 8255A device

Applications

The C8255A core is used to facilitate Processor I/O.

AllianceCORE™ Facts

Core Specifics	
See Table 1	
Provided with Core	
Documentation	Core documentation
Design File Formats	.XNF Netlist VHDL Source RTL
Constraint Files	.ncf
Verification Tool	Testbench, vectors
Schematic Symbols	Viewlogic
Evaluation Model	None
Reference designs & application notes	None
Additional Items	None
Design Tool Requirements	
Xilinx Core Tools	Alliance/Foundation 1.4
Entry/Verification Tool	1076-compliant VHDL simulator
Support	
Support provided by CAST, Inc.	

Figure 1: Core Implementation Data

CPLD	Macrocells[2]	Product Terms[2]	I/O[1]	Performance[2,3] (MHz)	Speed Grade
XC9500	109	434	38	76.9	-7
XC9500XL	105	413	38	100	-5
FPGA	**CLBs**	**Global IOBs**	**IOBs[1]**	**Performance (MHz)**	**Speed Grade**
XC4000XL	77	0	38	32.6	-09
Spartan	77	0	38	29.5	-3

Notes:
1. Assuming all core I/O are routed off-chip.
2. CPLD figures stated are for density-optimized place and route run through version 1.5 of Xilinx tools.
3. Performance figures are device speeds since core has no system clock.

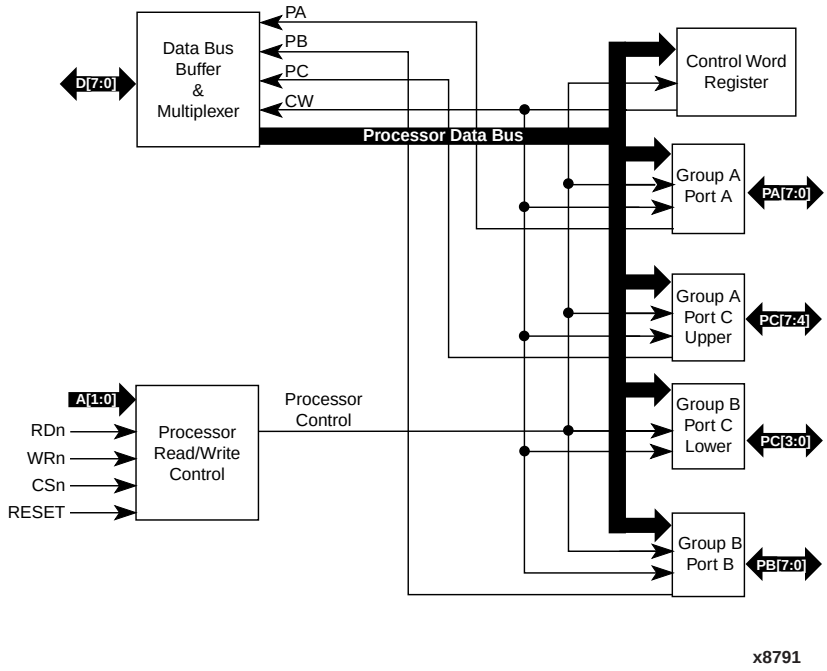

Figure 1: C8255A Peripheral Interface Block Diagram

General Description

The C8255A core is a general purpose programmable I/O device. It has 24 I/O pins programmable in 2 groups of 12 using 3 major modes. These modes allow the C8255A to be programmed in various ways to combine these pins as input, output or bi-directional ports.

Functional Description

The C8259A core is partitioned into modules as shown in Figure 1 and described below.

Data Bus Buffer and Multiplexer

The Data Bus Buffer and Multiplexer block interfaces the C8255A to the system Data Bus. Internally, this block multiplexes the peripheral busses PA, PB and PC.

Processor Read/Write Control

This block manages the internal and external transfers. It sets up and controls all of the Control Groups (Data Ports).

Control Word Register

The Control Word is the register which contains the programming of the C8255A.

Group A Port A

This block comprises the controls and buffer for Port A. Port A is a single 8 bit port and is entirely in group A.

Group A Port C (upper)

This block comprises the controls and buffer for the upper half of Port C. Port C has 4 bits in group A.

Group B Port B

This block comprises the controls and buffer for Port B. Port B is a single 8 bit port and is entirely in group B.

Group A Port C (lower)

This block comprises the controls and buffer for the lower half of Port C. Port C has 4 bits in group B.

Core Modifications

Additional ports can be added to this core by modifying the source code. Since the Xilinx netlist version of the core is not modifiable by the user, you would either need to purchase the source code version of this core or have CAST perform the modifications for you. Contact CAST directly for additional information.

Pinout

The pinout of the C8255A core has not been fixed to specific FPGA I/O, allowing flexibility with a user's application. Signal names are shown in the block diagram in Figure 1 and in Table 1.

Core Assumptions

Pull-up/Pull-down Bus Hold Devices

The Intel 8255A supports pull-up and pull-down bus hold devices on Port A and pull-up bus hold devices on Ports B and C. The C8255A model does not model this capability. On devices with pull-up resistors attached to I/O, the pull-up can be emulated. Otherwise external pull-up or pull-down resistors can be used.

System Data Bus Writes - Hold Time

The Intel 8255A-2 Address and Chip Select Hold Time After WRn Rising Edge is 20 ns minimum. On the C8255A model, the Address Hold Time (determined by the implementation technology) is with respect to WRn or CSn rising edge, which ever occurs first. That is to say, on system data bus writes, data will be captured on the rising edge of WRn or CSn, whichever occurs first.

Control Register Reads

The Intel 8255A does not support Control Register Reads by way of the system data bus. The C8255A does. On power-up reset, a read of this register yields 9B hexadecimal.

Control Register Writes and Device Reset

The Intel 8255A resets when the Control Register is programmed. The reset takes place with the WRn strobe's rising edge. The C8255A resets when the Control Register is programmed, but the reset takes place on the WRn strobe's low level. Note that a write to the Intel 8255A resets all ports and that the device was not designed for on-the-fly reprogramming.

Verification Methods

The C8255A core's functionality was verified by means of a proprietary hardware modeler. The same stimulus was applied to a hardware model which contained the original Intel 8255A chip, and the results compared with the core's simulation outputs.

Recommended Design Experience

The user must be familiar with HDL design methodology as well as instantiation of Xilinx netlists in a hierarchical design environment.

Table 2: Core Signal Pinout

Signal	Signal Direction	Description
D[7:0]	In/Out	Data Bus
A[1:0]	Input	Address
RDn	Input	Read Control
WRn	Input	Write Control
CSn	Input	Chip Select
RESET	Input	Reset
PA[7:0]	In/Out	Port A
PC[7:0]	In/Out	Port B
PB[7:0]	In/Out	Port C

Ordering Information

This product is available from CAST Inc. Please contact CAST Inc. for pricing and more information.

The C8255A core is licensed from Moxsyn S.R.L.

Related Information

Intel Peripheral Components Data Book

Intel order number: 296467
ISBN: 1-55512-127-6
Document number: 231308-002

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