IEEE 1394 FireWire Link Layer Core

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Features

- General Purpose LINK Layer Core
- Compliant with IEEE 1394-1995 specification
- Adaptable to most Isochronous 1394 Applications
- Annex J compliant interface between LINK and PHY
- Supports 1394 ISO Transmit and Cycle Master Receive transactions
- Supports speeds of 100 and 200 Mbits/sec
- Interface to standard V3 V292PBC-33LP PCI bridge chip local bus
- Additional options available extra from I²P
  - Optional verification environment
  - Optional Engineering Services
  - Optional software drivers for various applications

Applications

The core can be used in multimedia applications that require streaming audio or video data.

General Description

The I²P SuperLINKCore™ is a FireWire IEEE 1394 LINK Layer core designed to support isochronous transmission devices. The core is fully tested and verified according to the IEEE 1394-1995 specification. The core interfaces to a PCI Bridge Chip (V292PBC-33LP) from V3 Semiconductor, Inc.

AllianceCORE™ Facts

Core Specifics	
Device Family	XC4000XL-09
CLBs Used	886
IOBs Used	53[1]
System Clock f_{max}	50 MHz
Device Features Used	SelectRAM, LogiBLOX
Provided with Core	
Documentation	User Guide System Model User Guide
Design File Formats	Verilog compiled XNF netlist, .NGO file
Constraint Files	User constraints (.ucf) file
Verification Tool	Available extra
Schematic Symbols	None
Evaluation Model	None
Reference designs & application notes	None
Additional Items	None
Design Tool Requirements	
Xilinx Core Tools	Foundation M1.4
Entry/Verification Tool	FPGA Express
Support	
Support provided by Integrated Intellectual Property, Inc.	

Note:
1. Assuming all core signals are routed off-chip.

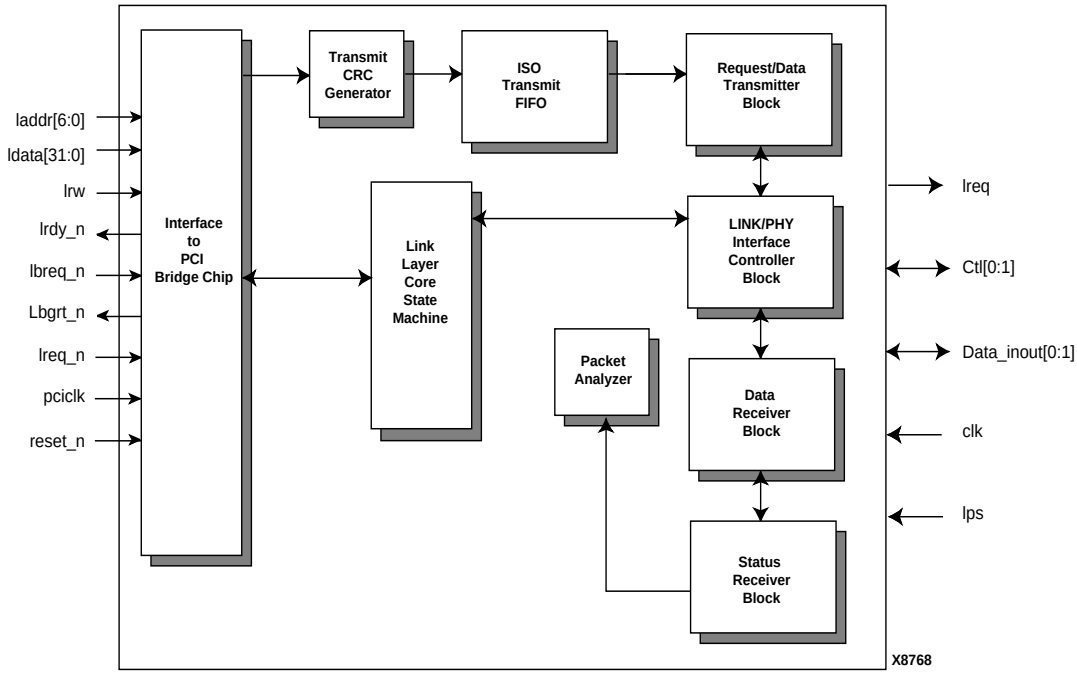

Figure 1: IEEE 1394 FireWire Link Layer Core Block Diagram

Functional Description

The core is compliant with the IEEE 1394-1995 specification. It has an Annex J compliant interface to the PHY layer and is designed in a highly modular fashion.

Interface to PCI Bridge Chip

This block is responsible for data transfers between the LINK core and the V3 PCI bridge chip. The core interfaces directly to the simple local bus provided on the backend of the V3 bridge chip. The customer's logic can initiate or receive 1394 packets with a very simple read/write protocol on the application interface.

Transmit CRC Generator

This generates a CRC on the transmitted packets.

ISO Transmit FIFO

This stores the 1394 ISO packets in the LINK layer.

Request/Data Transmitter Block

This generates the Local Request (lreq) and then sends the data to PHY on the Link/PHY interface.

Data Receiver Block

This is responsible for receiving data from the PHY and presenting it to the internal LINK logic. Currently, the data receiver module is capable of receiving cycle start packets from a root node and responding to it by sending ISO packets stored in the FIFO.

LINK Layer Core State Machine

This block is responsible for the generating the control signals for all modules in the core. It controls the overall functionality of the core.

Status Receiver Block

This receives the status information sent from the PHY layer and presents it to the internal LINK logic.

Link/PHY Interface Controller Block

This is responsible for generating control signals for the transmitter and receiver blocks. Additional 1394 transaction layer functions can also be incorporated.

Core Modifications

I²P can provide the following modifications to the core for additional cost above the netlist version of the core. Likewise, users can perform these modifications themselves by purchasing the source code version.

- Alternate host interfaces.
- Additional 1394 transaction layer functions.

Pinout

The pinout of the SuperLINKCore™ has not been fixed to specific FPGA I/O, allowing flexibility with a user application. Signal names are shown in the block diagram in Figure 1, and in Table 1.

Verification Methods

The core is fully tested and verified according to the IEEE 1394-1995 specification using the I²P verification environment. It has also been tested in hardware using a Xilinx FPGA-based evaluation board (see Available Support Products).

Recommended Design Experience

Knowledge of the IEEE 1394 specification is required. The user must be familiar with HDL design methodology as well as instantiation of Xilinx netlist in a hierarchical design environment.

Available Support Products

I2P supplies a complete line of hardware and software products designed to aid in the integration of this core into your application. These are available at additional cost. Contact I²P for more information.

- Xilinx FPGA-based IEEE 1394 FireWire hardware evaluation board.
- A complete IEEE 1394 verification environment is available for testing LINK or PHY designs. It includes features for automatic test generation, automatic topology setup and a complete verification checklist.
- Synthesizable Verilog source code version of the SuperLINKCore™ with synthesis scripts for a bottom-up hierarchical compile and user's guide.

Ordering Information

The core and products referenced in this product description are available directly from Integrated Intellectual Property, Inc. Contact them for pricing or additional information.

Related Information

1394 Trade Association

The 1394 Trade Association publishes the IEEE 1394 specification, and provides information for developers as well as related industry contacts and activities. For more information, contact them directly:

1394 Trade Association
URL: www.firewire.org or www.1394ta.org

Table 1: Core Signal Pinout

Signal	Signal Direction	Description
LINK to PCI Interface Signals		
laddr[6:0]	Input	Local bus address
ldata[31:0]	Input	Local bus Data
lrw	Input	Local bus read/write
lrdy_n	Output	Local bus ready
lbreq_n	Input	Local bus request
Lbgrt_n	Output	Local bus grant
lreq_n	Input	Local request
pciclk	Input	PCI clock (33 MHz)
reset_n	Input	PCI reset
LINK to PHY Interface Signals		
lreq	Output	Link request
Ctl[0:1]	In/Out	Control signals
Data_inout [0:1]	In/Out	Data signals
clk (50 Mhz)	Input	Link clock (50 MHz)
lps	Output	Link power status

V3 Semiconductor, Inc.

For additional information on the V3 V292PBC-33LP PHY chip, contact:

V3 Semiconductor, Inc.
URL: www.vcubed.com

Xilinx Programmable Logic

For information on Xilinx programmable logic or development system software, contact your local Xilinx sales office, or:

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