February 8, 1998 Product Specification

GV & Associates, Inc.

GV & Associates, Inc.

23540 Oriente Way
Ramona, CA 92065 USA
Phone: +1 760-789-7015
Fax: +1 760-789-7015
E-mail: gvander@sd.cts.com

Features

- 40 MHz maximum input A/D sample rate
- On-board 40 MHz Direct Digital Synthesizer
- 15 MHz sample Bandwidth
- FPGA Logic Expansion (from 13K gates to 100K gates)
- 40 MHz TI TMS320C541 DSP Processor
- 128K X 16 Flash EPROM
- 64K X 16 SRAM
- RS232 Serial Port
- FPGA Access to DSP Processor SRAM
- DSP Processor Interface to FPGA
- 24 bit FPGA Local Bus
- Xilinx FPGA Processor Peripheral, Master Parallel and Download Cable Configurations supported
- 40 MHz maximum output D/A sample rate
- Stereo Audio Amplifier with Stereo Jack
- Selectable 3.3V source for Xilinx FPGAs
- Programmable A/D Sample Clock
- Programmable DDS Sample Clock

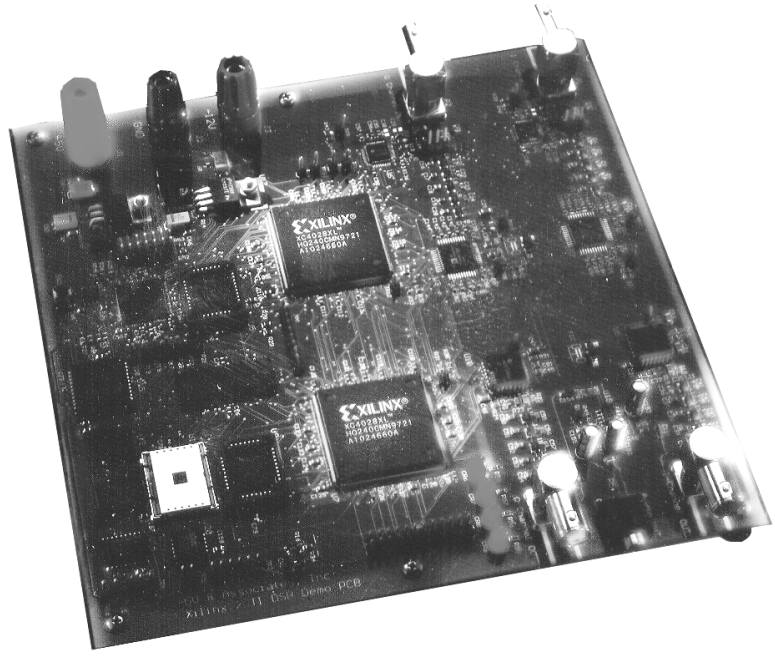

Figure 1: GVA-100 DSP Prototyping Platform

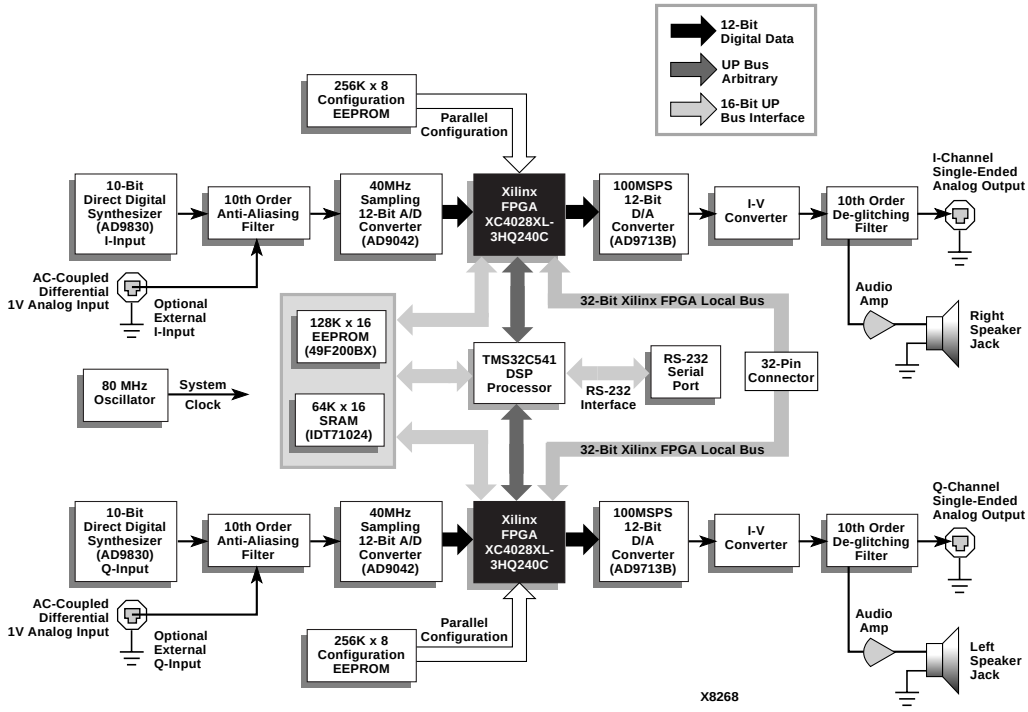

Figure 2: GVA-100 Block Diagram

General Description

The GVA-100 Digital Signal Processing Prototyping Platform is designed for testing complex DSP or other channel coding designs. This prototyping platform provides a highly flexible tool for testing various software and hardware DSP applications using the Xilinx XC4000 family.

The GVA-100 Supports the following Xilinx FPGAs:

- XC4013E-3PQ240C
- XC4020E-3PQ240C
- XC4025E-3PQ240C
- XC4028XL-3HQ240C
- XC4036XL-3HQ240C
- XC4044XL-3HQ240C
- XC4052XL-3HQ240C
- XC4062XL-3HQ240C

Functional Description

The platform's general configuration consists of an I and Q channel which pass through a 10th order low pass filter. The 10th order low pass filter band limits the input signals to a 15 MHz bandwidth. The signal rejection is -60 dB at 25 MHz. Next, the signals are digitized by a 12 bit A/D. The sample rate (maximum of 40 MHz) of the A/D is programmable since it is generated by the Xilinx FPGA. The digitized signals are then ready to be processed by the customer's algorithm which could be implemented in hardware by the Xilinx FPGA and/or in software by the TI TMS320C541 DSP Processor.

The digitized data may be accessed by the DSP Processor via the microprocessor / Xilinx bus interface. Once the signals have been processed, they are converted back to an analog waveform by a 100 MSPS D/A via the Xilinx FPGA. The processed analog waveforms are passed through a 10th order de-glitching filter which is band limited to 15 MHz. The de-glitched analog signal is passed to a 50 ohm BNC output for viewing and to an audio amp which may be accessed via the stereo jack.

Additionally, Direct Digital Synthesizers (DDS) on each channel provide the option for an on-board signal source. The DDS can be programmed by the FPGA or the DSP Processor via the microprocessor address/data bus interface. The clock rate of the DDS is programmable since it is generated by the FPGA.

The FPGA may access the Processor memory (SRAM) through the bus arbitration circuitry of the TMS320C541. Also, the two Xilinx FPGAs have a 32 bit local bus which allows for the direct transfer of data between the two devices. This could be used as direct digital data port or as a data transfer path between both FPGAs to implement the desired DSP algorithm.

Ordering Information

This product is available directly from GV & Associates. Please contact them for pricing and more information.

Related Information

For information on Xilinx programmable logic or development system software, contact your local Xilinx sales office, or:

Xilinx, Inc.
2100 Logic Drive
San Jose, CA 95124
Phone: +1 408-559-7778
Fax: +1 408-559-7114
URL: www.xilinx.com

For general Xilinx literature, contact:

Phone: +1 800-231-3386 (inside the US)
+1 408-879-5017 (outside the US)
E-mail: literature@xilinx.com

For AllianceCORE™ specific information, contact:

Phone: +1 408-879-5381
E-mail: alliancecore@xilinx.com
URL: www.xilinx.com/products/logicore/alliance/tblpart.htm