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## Features

- Drop-in modules for the XC4000E, EX, XL, XV and Spartan families
- Two data bus inputs: 2 to 30 bits wide
- Supports both 2's complement signed and unsigned data
- Registered output
- Load feature to directly load the output register
- Clock Enable for output register
- Asynchronous Clear for output register
- Uses Fast Carry logic for high speed
- High performance and density guaranteed through Relational Placed Macro (RPM) mapping and placement technology
- Available in Xilinx CORE Generator

## Functional Description

The Registered Loadable Subtractor module accepts two input buses, **A** and **B**, and a borrow input (**CI**), subtracts **B** and **CI** from **A**, and registers the result, **S**. The input data buses can be in either 2's complement signed or unsigned numbers.

The borrow input is active low, but is otherwise interpreted as a 1-bit binary value.

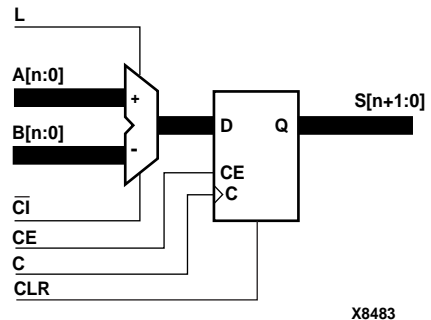
The output bus width is automatically set to the input bus width plus 1 to accommodate any borrow that may be produced when subtracting the MSB's of the input operands.

When the Load (**L**) and Clock Enable (**CE**) signals are asserted, the **B** input data bus is loaded directly into the output register on the rising edge of the Clock.

Since the output bus is 1-bit wider than the B input bus, when data is loaded into the register (**L**=HIGH), the additional bit in the output bus - the MSB - is set to 0 if unsigned data is selected, or is assigned the same value as the MSB of the B input bus if signed data is selected.

## Pinout

Signal names for the schematic symbol are shown in Figure 1 and described in Table 1.



X8483

Figure 1: Core Schematic Symbol

Table 1: Core Signal Pinout

Signal	Signal Direction	Description
L	Input	LOAD – active high signal bypasses the subtractor and directly loads the B data into the output register.
A[n:0]	Input	A data input ignored when Load (L) is active.
B[n:0]	Input	B data input – value is subtracted from A data along with the borrow input (CI).
$\bar{C}I$	Input	BORROW IN – Active Low, ignored when Load (L) is active. Treated as a 1-bit binary number and subtracted from A.
CE	Input	CLOCK ENABLE – active high signal used to enable the transfer of data from the subtractor or the B input to the output register.
C	Input	CLOCK – with the exception of asynchronous control inputs (where applicable), control and data inputs are captured, and new output data formed on rising clock transitions.
S[n+1:0]	Output	DATA OUTPUT – the registered output of the subtractor. Note: 1-bit wider than input operands.
CLR	Input	ASYNCHRONOUS CLEAR - resets the output register. Overrides Clock and Clock Enable. Level sensitive.

## CORE Generator Parameters

The CORE Generator parameterization window for this macro is shown in Figure 2. The parameters are as follows:

- **Component Name:** Enter a name for the output files generated for this module.
- **Input Width:** Select an input bit width from the pull-down menu. The valid range is 2-30. The same data width is applied to both the A and B inputs. The output size is automatically set to the input width plus one.
- **Signed:** Select Signed or Unsigned.

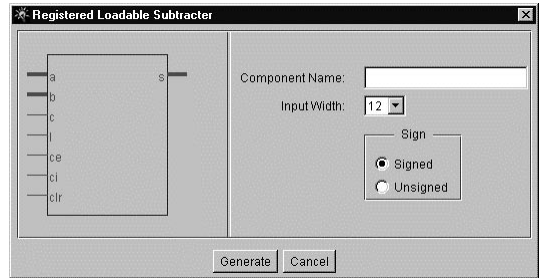


Figure 2: Parameterization Window

## Core Resource Utilization

Table 2 shows the number of CLBs required for each available bit width.

## Ordering Information

This macro comes free with the Xilinx CORE Generator. For additional information contact your local Xilinx sales representative, or e-mail requests to [coregen@xilinx.com](mailto:coregen@xilinx.com)

**Table 2: Bit Width versus CLB Count**

Bit Width	CLB Count
2	2
3	2
4	3
5	3
6	4
7	4
8	5
9	5
10	6
11	6
12	7
13	7
14	8
15	8
16	9
17	9
18	10
19	10
20	11
21	11
22	12
23	12
24	13
25	13
26	14
27	14
28	15
29	15
30	16

**Parameter File Information**

Parameter Type	Type	Notes
Component_Name	String	
Input_Width	Integer	2 - 30
Signed	Boolean	True/False

