Pipelined Delay Element

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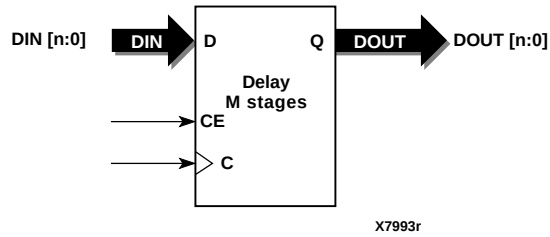

Figure 1: Core Schematic Symbol

Features

- Drop-in modules for the XC4000E, EX, XL, XV and Spartan families
- Uses highly area efficient SelectRAM™ for storage
- Delay selectable from 1 to 600 clock cycles
- Data widths from 2 to 32
- Clock Enable for internal registers
- High performance and density guaranteed through Relational Placed Macro (RPM) mapping and placement technology
- Available in Xilinx CORE Generator

Functional Description

This module implements an M-stage by N-bit delay by storing data samples in a 16-word by N-bit wide SelectRAM™. If more than 17 delay stages are required (16-word deep SelectRAM™ plus one register) multiple 16-word RAMs are used. Each 16-word, N-bit RAM requires N/2 XC4000 series FPGA configurable logic blocks (CLBs) for even N and N/2 + 1 CLBs when N is odd.

Typical applications include synchronization of multiple data paths in DSP applications as they go through filtering and other signal processing.

Pinout

Port names for the schematic symbol are shown in Figure 1 and described in Table 1.

Table 1: Core Signal Pinout

Signal	Signal Direction	Description
DIN[n:0]	Input	PARALLEL DATA IN
CE	Input	CLOCK ENABLE - active high. DOUT port only changes when CE is active. Data new in the delay line is unaffected by clock edges when CE is inactive.
C	Input	CLOCK - with the exception of asynchronous control inputs (where applicable), control and data inputs are captured, and new output data formed on rising clock transitions.
DOUT[n:0]	Output	PARALLEL DATA OUT - DIN delayed by M clock cycles.

CORE Generator Parameters

The CORE Generator parameterization window for this macro is shown in Figure 2. The parameters are as follows:

- **Component Name**: Enter a name for the component.
- **Port Width**: Select an input bit width from the pull-down menu. The valid range is 2-32.
- **Pipeline Stages:** 1 to 600 stages may be defined.
- **Create RPM:** When checked the CORE generator adds placement information to the module. Alternatively if left unchecked the place and route software may place each CLB independently. RPMs usually result in higher performance and faster implementation times.

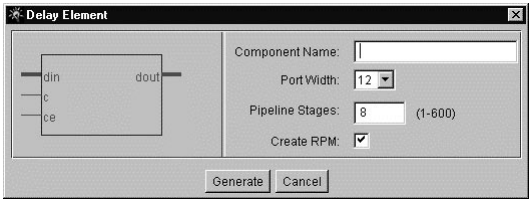

Figure 2: Parameterization Window

Core Resource Utilization

Tables 2 and 3 show the number of CLBs required for bit widths from 2 to 17 and delays from 1 to 17.

Table 2: Utilization for Delays Between 1 and 4 Inclusive

Data Bit Width	CLB Count
2	2
3	3
4	3
5	4
6	4
7	5
8	5
9	6
10	6
11	7
12	7
13	8
14	8
15	9
16	9
17	10

Table 3: Utilization for Delays Between 5 and 17 Inclusive

Data Bit Width	CLB Count
2	4
3	5
4	5
5	6
6	6
7	7
8	7
9	8
10	8
11	9
12	9
13	10
14	10
15	11
16	11
17	12

Ordering Information

This macro comes free with the Xilinx CORE Generator. For additional information contact your local Xilinx sales representative, or e-mail requests to coregen@xilinx.com.

Parameter File Information

Parameter Name	Type	Notes
Component_Name	String	
Port_Width	Integer	2 - 32
Pipeline_Stages	Integer	1 - 600
Create_RPM	Boolean	True/False