LogiCORE™ Xilinx CORE Generator

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The Xilinx CORE Generator is an FPGA productivity enhancement tool that generates parameterized building blocks (cores) compatible with standard Xilinx FPGA design methodologies.

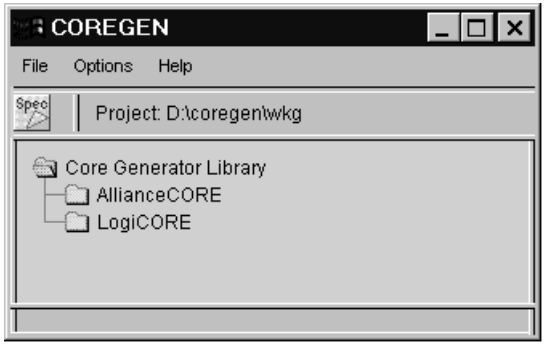

Figure 1: The CORE Generator Window

Features

- Compatible with VHDL, Verilog, and schematic capture top-level design methodologies.
- Supports PC and Workstation platforms and permits web-based operation.
- Supports Xilinx LogiCOREs and third-party AllianceCOREs.
- Easy to use, intuitive point and click operation.
- Plug & Play-COREs can be added at any time by downloading new cores from the Xilinx web page.
- Supplies the link from system level design tools to Xilinx FPGA silicon.
- Compatible with Xilinx Foundation, Alliance, and XACT development systems.

CORE Generator with Xilinx LogiCOREs

- Automatically generates parameterized cores and HDL behavioral models.
  - Wide range of core complexity from basic logic building block to system level functions.
  - Supports the XC4000E, EX, XL, XV, and Spartan FPGA families.
- Unique methodology produces a logic design and a layout (floorplan) for each core.
- Generates optimal designs (best performance and density) for FPGAs.
- Performance and size are known and specified before the core is generated.
- Consistent performance independent of Xilinx FPGA device size and independent of percent utilization.
- Reduces overall FPGA implementation time; cores come mapped and relatively placed.

Introduction

The Xilinx CORE Generator generates parameterized cores optimized for Xilinx FPGAs. It serves as a cataloging and delivery vehicle for Xilinx designed and supported LogiCOREs, third-party designed and supported AllianceCOREs, data sheets, and application notes.

The CORE Generator fills the need created by the introduction of the next generation high-capacity FPGAs that use advanced semiconductor process technology. A 100,000-gate design can be built from a collection of cores in a matter of hours.

FPGA LogiCORE: Matrix of CLBs

Xilinx FPGAs consist of an expandable matrix of “Configurable Logic Blocks” (CLBs). A LogiCORE is delivered as a pre-defined group of CLBs that maintain their relative locations when placed anywhere in an FPGA.

Unique Design Methodology: CORE Generator and LogiCOREs

The output of the CORE Generator is a netlist that specifies the logic design and a physical layout or floorplan. This logic and layout methodology, combined with the segmented routing architecture of the Xilinx XC4000 family, generates designs with guaranteed performance. The size (number of CLBs) and the performance (maximum operating frequency) are specified in the data sheet for each core.

When installed in an FPGA, the cores meet the same performance specifications independent of device size and

independent of how many cores are used in a large FPGA device.

Traditionally, cores for most other FPGAs are “soft” cores because the physical layout and characteristics of the design cannot be known prior to placement and routing. Every placement and routing iteration results in a different physical layout and as a result, the performance is not predictable.

The CORE Generator takes advantage of the Xilinx segmented architecture and does not use any of the global routing resources except for the global clock distribution network. The core can be placed anywhere in any size FPGA and then interconnected with standard routing software. The performance will always be the same for a given speed device.

Without this predictability it is not possible to know whether a design will work until the final phases of a project, when it may be too late to move to an alternative approach. With the CORE Generator approach, the theoretical design matches the actual design.

Designs optimized for FPGAs

The CORE Generator produces designs that are optimized for FPGAs in two ways. First, the LogiCORE implementations are generated with FPGA architecture in mind and take advantage of the look-up table logic and distributed RAM. Second, they include mapping information and relative location constraints for each CLB so that the layout (floorplan) is always optimal.

The efficiency (number of CLBs) and performance of each parameterized LogiCORE is comparable to a hand-packed design.

The FPGA device power dissipation is also improved through the use of cores. Designs with optimal layout use less programmable interconnect and thus less dynamic power.

Compatible with standard tools

The CORE Generator can be used with any HDL top-level design methodologies or schematic capture design tools (Xilinx Foundation or Viewlogic).

For HDL environments the CORE Generator produces VHDL or Verilog code that can be spliced into the top-level HDL design. This instantiation code directs the synthesis tool to the associated core netlist during the HDL synthesis process and the Xilinx place and route tools combine all of the netlists into a single design. The CORE Generator also delivers a behavioral model for simulation.

For schematic capture flows a symbol is automatically generated. The user-parameterized core can then be included in the overall schematic along with traditional schematic elements.

CORE Generator Design Flow

When the Xilinx CORE Generator is initiated, a COREGEN window appears with expandable folders that contain lists of available cores and lower level functional building blocks. The hierarchical list can be expanded until the desired core is located and its parameterization screen appears. Enter the parameters and click on the generate button to initiate the core generation process.

After the parameterized core is generated, the schematic symbol is placed in the schematic capture library or the HDL instantiation code is placed in a file.

The parameterized core can be used with either Foundation or Alliance series flows.