Dual Port Block RAM

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Features

- Supports data widths up to 512 bits
- Supports memory depths up to 4096 words
- Allows power-on memory content to be defined
- Uses Virtex™ block memory for performance and efficiency
- Two access ports permit simultaneous read/write operations to common memory pool
- Simultaneous access to same location permitted
- Memory dimensions of each memory access port independently configurable
- Fully synchronous
- Drop-in modules for the Virtex™ family
- Available in Xilinx CORE Generator

Functional Description

The Dual Port Block RAM has two independent access ports that permit shared access to a central pool of memory. The data width and memory depth of each access port can be independently configured providing straightforward dual-port memory functionality, or optional data-formatting capability.

Both ports are functionally identical, with each port providing read and write access. Simultaneous reads from the same memory location may occur, but all other simultaneous, same-location operations should be avoided. Simultaneously reading-from and writing-to the same location results in the correct data being written into memory but invalid data being presented at the reading port.

Access port A takes an N-bit data value and an M-bit address, and access port B takes a Q-bit data value and a P-bit address. When both access ports are disabled (ENA=0 and ENB=0) the memory contents and output ports (DOA and DOB) remain unaltered. When an access port is enabled (ENA=1 or ENB=1) all memory operations occur on the rising edge of the respective port's clock input (CLKA or CLKB). During a write operation (WEA=1 or WEB=1) the data presented at the relevant port's data input (DIA or DIB) is stored in memory at the location selected by the relevant port's address input (ADDRA or ADDRB). If an access port is not in reset mode (RSTA=0 or RSTB=0) the data value(s) being written will also appear at the respective port's data output. During a read operation (WEA=0 and RSTA=0 or WEB=0 and RSTB=0) the contents of the addressed location(s) will appear at the port's data output(s). While in reset mode (RSTA=1 or RSTB=1) the port's data output is held LOW, although memory write operations may still take place. (Simply asserting RSTA or RSTB has no effect on memory contents.)

The initial contents of the memory (i.e. the data stored in the memory immediately after device configuration) may also be specified.

Pinout

Port names for the core module are shown in Figure 1 and described in Table 1.

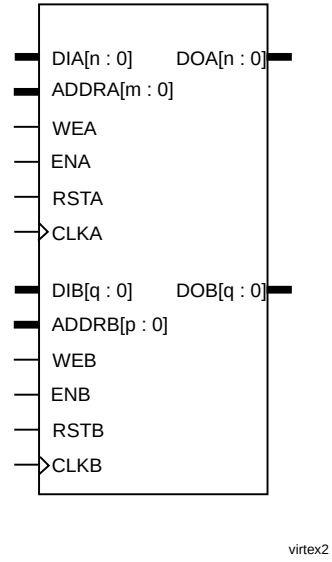

Figure 1: Core Schematic Symbol

Table 1 : Core Signal Pinout

Signal	Signal Direction	Description
DIA[n:0]	Input	PORT A DATA INPUT - data to be written into memory via port A
DIB[q:0]	Input	PORT B DATA INPUT - data to be written into memory via port B
ADDRA[m:0]	Input	PORT A RAM ADDRESS - the memory location to which data will be written or from which data will be read via port A
ADDRB[p:0]	Input	PORT B RAM ADDRESS - the memory location to which data will be written or from which data will be read via port B
WE[A|B]	Input	PORT A|B WRITE ENABLE - active high signal used to allow transfer of data into memory via port A or port B
EN[A|B]	Input	PORT A|B ENABLE - active high signal used to allow read/write or reset mode operations to take place within the memory via port A or port B.
RST[A|B]	Input	PORT A|B RESET - active high signal used to force the module's outputs LOW. Does not affect memory contents.
CLK[A|B]	Input	PORT A|B CLOCK - when Block RAM is enabled, control and data inputs are registered, and new output data formed on the rising clock edge
DOA[n:0]	Output	PORT A DATA OUTPUT - when access port A is enabled (ENA=1) this port reflects the data stored at the location selected by the ADDRA address. Low when RSTA is asserted. When access port A is disabled, maintains the previous value. Low when RSTA is asserted.
DOB[q:0]	Output	PORT B DATA OUTPUT - when access port B is enabled (ENB=1) this port reflects the data stored at the location selected by the ADDRB address. Low when RSTB is asserted. When access port B is disabled, maintains the previous value.

CORE Generator Parameters

The CORE Generator parameterization window for this macro is shown in Figure 4. The parameters are as follows:

- **Component Name:** Enter a name for the output files generated for this module.
- **Port A**
  - **Depth:** Select the number of words in the RAM from the pull down menu.
  - **Data Width:** Select the input bit width from the pull down menu. The entries in this field are constrained by the value entered in the depth field. Table 2 illustrates the relationship between depth and width.
  - **Address Width:** Shows the number of bits needed to address all of the locations in the Block RAM. This field is read only.
- **Port B (constrained by Port A Values)**
  - **Depth:** Select the number of words in the RAM from the pull down menu. This is constrained to factors of the Port A depth which are an integer power of 2. Entries in this field will influence the available entries in the Port B data width field.
  - **Data Width:** Select the input bit width from the pull down menu. The entries in this field will be constrained by the values of the Port A depth and data-width fields. Entries in this field will influence the available entries in the Port B depth field.

- **Address Width:** Shows the number of bits needed to address all of the words in the Block RAM. This field is read only.

- **Blocks*:** Shows the number of Block RAM primitives required to implement a memory with the requested dimensions. Table 2 also shows this information. This field is read only.
- **Load Init Values:** Specifies the file that contains the initial values for the Block RAM.
- **Show Invalid Values:** Display any initial values that are invalid for use in the specified Block RAM, after they have been loaded.
- **coe file:** Displays the name of the coefficient file. This field is read only.

*Note: Ensure that the target device has sufficient memory blocks to accommodate the specified memory, including any memory blocks used elsewhere in your application. Table 2 shows how many memory blocks are available in each device.

Dissimilar Port Dimensions

The dimensions (depth and width) of access port A and access port B do not have to be the same. While the depth of both port A and port B must be one of the values 256, 512, 1024, 2048, or 4096, the depth of port B may be equal-to or less than the depth of port A.

In the case where the depth of both ports is identical, the data width of both ports will be identical also. However, when the depth of port B is set to a value that is less than the depth of port A, the data width of port B will be proportionately greater than port A. For example, choosing a depth for port B that is a quarter the depth of port A will result in a data width for port B that is four times that of port A.

Since each port is accessing the same quantity of memory, data words formatted appropriately for port B will be equivalent to one or more data words formatted for port A. The example shown in Figure 2 illustrates a Block RAM configured with access port A describing a 1024 word by 16 bit memory, and access port B describing a 256 word by 64 bit memory. A single memory access to port B is equivalent to four accesses made to port A.

Specifying Memory Contents

The initial contents of the Block RAM can be assigned, with respect to Port A, by specifying the desired information in a text file - known as a COE file. In addition to the initial memory contents, all the parameters visible on the parameterization window may be assigned values in the COE file. COE files may take any root file name but must end with the extension ".coe".

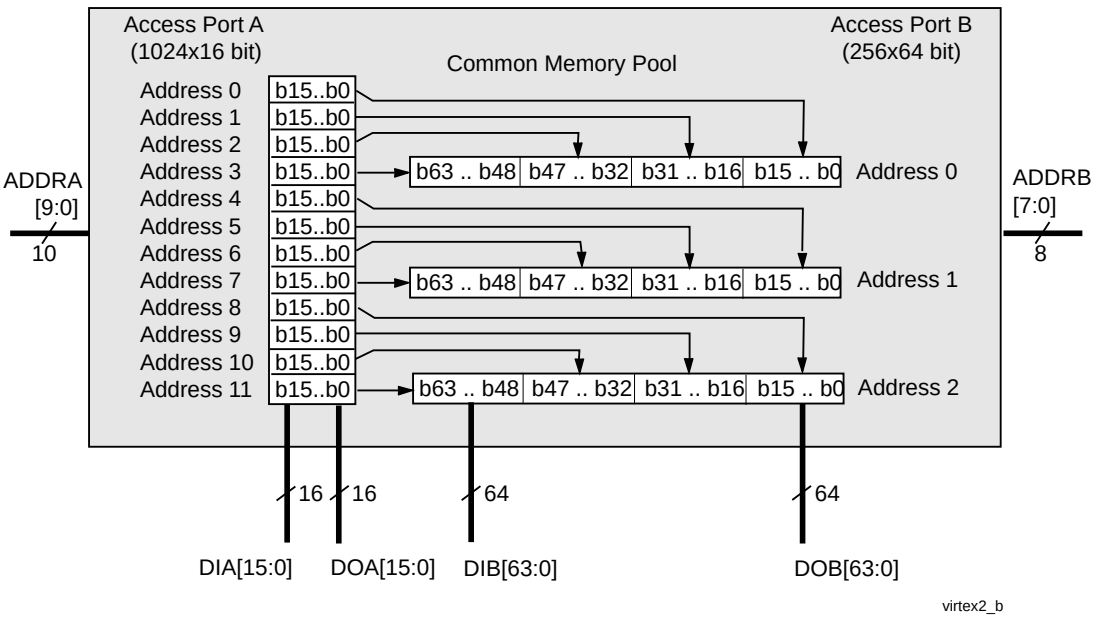

Figure 2: Relationship Between Dissimilar Access Port Dimensions

To select and load a COE file, press the "Load Init Values..." button on the parameterization window and choose the desired file from the dialog-box. Any field on the parameterization window that is assigned a value in the COE file will lose its previous value when the COE file is loaded. Changing a parameter value that was previously loaded from a COE file causes the COE file's name to be highlighted in red, indicating that the settings have changed since the file was loaded. If any of the initialization values are inconsistent with the other Port A parameters specified, an error is raised. The inconsistent data can then be reviewed by pressing the “Show Invalid Values…” button, which will now be highlighted in red.

For a detailed description of the COE file syntax, please refer to the Xilinx CORE Generator User Guide. The COE keywords supported by the Single Port Block RAM module, are shown in the Parameter File Information table at the end of this data sheet. An example COE file is shown below in Figure 3.

When specifying the initial contents for a memory in a COE file the keywords **DEFAULT_DATA**, **MEMORY_INITIALIZATION_VECTOR** and **RADIX** may be used. The **DEFAULT_DATA** keyword allows a value to be assigned to all memory locations with a single statement. If not set the **DEFAULT_DATA** value is 0. The **DEFAULT_DATA** value is overridden by the **MEMORY_INITIALIZATION_VECTOR** but only for the memory locations covered by the vector. The **MEMORY_INITIALIZATION_VECTOR** takes the form of a sequence of comma separated values, one value per memory location (consistent with port A's depth parameter), terminated by a semi-colon. Any amount of white space, including newlines, can be included in the vector to allow more readable data. The format of an individual value in the vector will depend on the **RADIX** value, which can be “2”, “10” or “16”, (the default value is 16). The vector values must be consistent with the **RADIX** value and must fall within the range 0 to $2^{PORT\_A\_DATA\_WIDTH}$-1. Values may not be negative.

Core Resource Utilization

The number of Block RAM primitives required to implement a particular memory is dependent on the values of the depth and data width fields selected in the CORE generator parameterization window and, for either Port A or B, is equal to:

(depth*data_width)/4096.

Table 2 specifies the number of blocks required for the allowable depth and data width values. The table also details the smallest device, in the Virtex family, that provides a particular number of primitives.

Table 2 : Block RAM Widths Available by Depth and Number of Blocks

	Memory Depth					Smallest
Blocks	**256**	**512**	**1024**	**2048**	**4096**	**Device**
1	16	8	4	2	1	
2	32	16	8	4	2	
3	48	24	12	6	3	
4	64	32	16	8	4	
5	80	40	20	10	5	
6	96	48	24	12	6	
7	112	56	28	14	7	
8	128	64	32	16	8	XCV50
9	144	72	36	18	9	
10	160	80	40	20	10	XCV100
11	176	88	44	22	11	
12	192	96	48	24	12	XCV150
13	208	104	52	26	13	
14	224	112	56	28	14	XCV200
15	240	120	60	30	15	
16	256	128	64	32	16	XCV300
17	272	136	68	34	17	
18	288	144	72	36	18	
19	304	152	76	38	19	
20	320	160	80	40	20	XCV400
21	336	168	84	42	21	
22	352	176	88	44	22	
23	368	184	92	46	23	
24	384	192	96	48	24	XCV600
25	400	200	100	50	25	
26	416	208	104	52	26	
27	432	216	108	54	27	
28	448	224	112	56	28	XCV800
29	464	232	116	58	29	
30	480	240	120	60	30	
31	496	248	124	62	31	
32	512	256	128	64	32	XCV1000

```
Component_Name =dpram;
Data_Width_A = 8;
Depth_A = 512;
Data_Width_B = 16;
Depth_B = 256;
Radix = 16;
Default_Data = FF;
Memory_Initialization_Vector = 12, 34, 56,
aa, aa;
```

Figure 3: An example COE file for a Dual Port Block

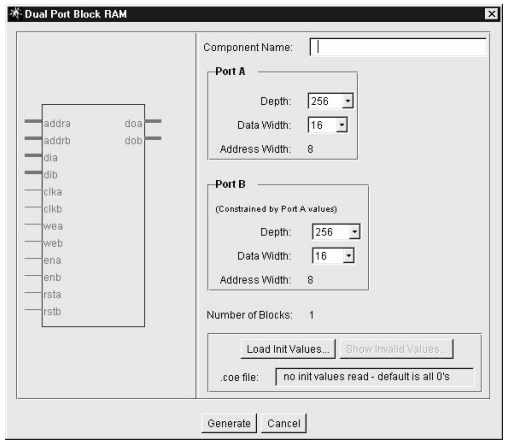

Figure 4: Parameterization Window

Ordering Information

This macro comes free with the Xilinx CORE Generator. For additional information contact your local Xilinx sales representative, or e-mail requests to coregen@xilinx.com .

Parameter File Information

Parameter Name	Type	Notes
Component_Name	String	
Depth_A	Integer	See Table 2
Depth_B	Integer	See Table 2
Data_Width_A	Integer	See Table 2
Data_Width_B	Integer	See Table 2
Default_Data	Integer	Value should be consistent with port A data width.
Memory_Initialization_Vector	Integer List	Comma separated and semi-colon terminated. Values should be consistent with port A data width and depth
Radix*	Integer	2,10 or 16

* COE file only