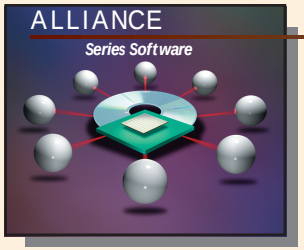

Xilinx Synplicity Information

FPGA	XC4000E XC4000X XC4000EX XC4000XLA	XC4000XV Spartan Spartan-XL Virtex
CPLD	XC9500	XC9500XL

Recommended Settings

For recommended settings, go to
http://www.xilinx.com
"Product"→"Software Solutions"

Xilinx Contacts and Technical Support

World Wide Web:
http://www.xilinx.com

North America	France
1-800-255-7778	33 1-3463-0100
hotline@xilinx.com	frhelp@xilinx.com
United Kingdom	Japan
44 1932-820821	81 3-3297-9163
ukhelp@xilinx.com	jhotline@xilinx.com

Synplicity Contacts and Technical Support

World Wide Web:
http://www.synplicity.com

E-mail	Telephone
support@synplicity.com	1-408-617-6000

HDL Library and Language Support

Synplify supports the synthesizable subsets of:
VHDL, Verilog HDL, IEEE 1076 -93, IEEE 1364 -95 Verilog HDL and 1164 VHDL
Libraries include: • Synplify library and attributes • std_logic_1164 & numeric_std • std_logic_arith • std_logic_signed • std_logic_unsigned • user-defined packages

Guide Overview

1 Invoke Synplify

Invoke the Synplify synthesis tool.
The Synplify Project Window is displayed listing Source Files, Result Files, and Target information.

2 Specify input files

Press the **right mouse button** in the Source Files list box and select **Add Source Files**.
Select Verilog or VHDL file(s) and **click OK**.
(See synplcty\examples for examples.) You can also add files from File Manager or Explorer into the Project Window by drag-and-drop.

Synplify chooses the last module compiled as the top-level module for Verilog designs. For VHDL designs, Synplify places the last architecture for the last entity within the last file compiled into Synplify.

3 Select target architecture & options

From the menu bar, choose **Target→Set Device Options...** and choose your target architecture and options and **click OK**.

4 Synthesize

Synplify accepts timing constraints for synthesis. Design constraints are passed on to the implementation tools. See the Synplify On-line help.

Click the **Run** button. Click the **View Log** button to View the Synplify Log file after Synplify shows **Done!** Double-click on the result file name to view the output file. Place and route the design.
Optional: Save this configuration in a Project File.

5 *Optional* Save recommended setting configuration in a Project File.

- Set the **Fanout Limit** at **100** *default*
- Turn on **Force GSR Usage** option *default*
- Turn on **Target M1 Place & Route** option *default*

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