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FOR IMMEDIATE RELEASE

XILINX AND MENTOR GRAPHICS ANNOUNCE STAMP SUPPORT FOR SYSTEM-LEVEL VERIFICATION

SAN JOSE, Calif., May 17, 1999—Xilinx Inc., (NASDAQ:XLNX) and Mentor Graphics Corporation, (NASDAQ:MENT) today jointly announced support for Stamp file format, bringing easy-to-use board-level timing verification capability to mainstream design engineers.

The industry-standard, Stamp file format output is generated by the new Xilinx Alliance Series software version 2.1i. The Mentor Graphics Tau™ 2.1 board timing verification software reads Stamp models. These models specify pin-to-pin timing delay and constraint information for components. Xilinx is the first PLD supplier to output the Stamp file format from its implementation software.

"Combined with our world class implementation tools, our CORE Generator, and the superior Virtex FPGAs, Xilinx has the complete solution for system-level integration," said Rich Sevcik, senior vice president software, cores, and support.

The Stamp format simplifies the design flow by using a single industry standard rather than multiple standards like SDF, structural Verilog and a technology library. Users no longer need to manage a library of standards and file formats. Additionally users no longer need to create component models from scratch—an arduous and time-consuming process. Because the Tau product can read Stamp models, board design engineers now have an automated solution for FPGA model generation. The close link between Xilinx and the Tau product is particularly important given the many revisions an FPGA goes through, and the need to have the most up-to-date timing information for accurate timing verification.

"This new capability from Xilinx will significantly shorten the time required to verify board timing," said Henry Potts, vice president and general manager of the Board Design Solutions Division at Mentor Graphics. "Combined with Tau, Xilinx Stamp support gives board designers the timing verification solution they need to deliver high-performance, reliable boards that work first time, on time."

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"Board timing verification is a very important step in our design process and we use Tau for this purpose. Also, the timing critical portion of our designs often contain Xilinx FPGAs," said Roger Yang, verification engineer at Cisco Systems. "For this reason, we requested Xilinx to provide pin-to-pin timing information for their FPGAs. The new Stamp model generation capability from Xilinx with both maximum and minimum delay data will greatly simplify the process of verifying FPGA timing as part of a board."

In addition to solving the modeling problem, Tau 2.1 software offers state-of-the-art analysis capabilities. The Tau product uses symbolic timing analysis technology to provide worst-case results in one pass and without false violations.

Symbolic analysis reasons over the functional information in component models to automatically eliminate the reporting of false timing violations. In addition, through its delay correlation capability, symbolic analysis accounts for the tracking of delay within components and correctly handles the "common ambiguity" problem. Tau 2.1 software performs clock tree analysis and computes the skew and phase shift between clocks, taking component and interconnect delay into account.

The SelectI/Os within the Virtex FPGAs enable system designers to interface with a variety of business standards for systems interfacing, general-purpose logic, high-speed SDRAM, and high-speed backplane driver applications, like LVTTL, LVCMOS2, PCI33, PCI66, GTL/GTL+, SSTL, HSTL, and CTT. Stamp models provide a methodology to accurately analyze systems on a board in a language that is widely industry-accepted.

About Mentor Graphics

Mentor Graphics is a world leader in electronic hardware and software design solutions, providing products and consulting services for the world’s largest electronic and semiconductor companies. Established in 1981, the company reported revenues over the last 12 months of $490 million and employs approximately 2,600 people worldwide. Company headquarters are located at 8005 SW Boeckman Road, Wilsonville, Oregon 97070-7777. World Wide Web site: http://www.mentor.com.

About Xilinx

Xilinx is the leading innovator of complete programmable logic solutions, including advanced integrated circuits, software design tools, predefined system functions delivered as cores, and unparalleled field engineering support. Founded in 1984 and headquarters in San Jose, Calif., Xilinx invented field programmable gate arrays (FPGA) and commands more than half of the world market for these devices today. Xilinx solutions enable customers to significantly reduce the time required to

develop products for the computer, peripheral, telecommunication, networking, industrial control, instrumentation, high-reliability/military, and consumer markets. For more information, visit the Xilinx web site at www.xilinx.com.

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