Frequently asked Questions and Answers

for Xilinx version 2.1 Software

What product configurations are available for the v2.1i development systems?

Xilinx offers its development systems in two series of products to match customer design requirements – The Alliance and Foundation Series software.

The Xilinx Alliance Series software is a state-of-the-art programmable logic development system that features advanced integration into the tool suites from Alliance Partners such as Exemplar, Mentor, Synopsys, and Synplicity.

The Foundation Series software provides a ready-to-use programmable logic design environment in a number of cost effective configurations. This environment includes Schematic and HDL design entry tools, ABEL, VHDL, and Verilog synthesis using Synposys FPGA Express, Xilinx 2.1i implementation tools, and a robust set of verification capabilities.

Who are the Xilinx Alliance partners?

Xilinx works closely with each of the leading EDA vendors to ensure high quality results when using third-party EDA tools with Xilinx advanced implementation tools. A full list of these partners is available at: www.xilinx.com/programs/alliance/alligen.htm#CAT

When will the v2.1i development systems ship to customers?

The first v2.1i-based product to ship will be the Xilinx Alliance Series product, available in June 1999. Foundation Series shipments will begin in July 1999.

What new features are there in the version 2.1i development systems?

Development efforts for the v2.1 software have been focussed on Internet enabled design capabilities including Internet Team Design (ITD) methods, compile time reductions, improvements to design clock speed, and continuing to improvement in productivity and ease-of-use.

The Xilinx Alliance Series products have a several unique capabilities that were added for the v2.1i release, including support for STAMP models, and Xilinx Internet Team Design capabilities.

The Xilinx Foundation Series is improved through the inclusion of Synopsys FPGA Express v3.2, better design flow automation, and the embedding of the Xilinx CORE Generator tool. Features that are specific to Synopsys® FPGA Express™ 3.2 release include the first production shipment of Vista™, the use of NCF for EDIF and XNF netlist flows, TCL scripting capabilities, and dramatic improvements in quality of result and runtime for designs, which include multipliers.

Some specific features added to the implementation tools—common to both Foundation Series and Alliance Series products—are:

- floorplanner support for the Virtex family
- fast, hierarchical browsing in timing analyzer
- CPLD ChipViewer tool for quick, graphical pin assignment and layout analysis
- FPGA Editor, including the probe capability for fast design debug in the lab
- new and improved constraints editor
- HTML-based documentation for quick browsing
- Synopsys LMG Smartmodel™ support for Virtex FPGAs

Further details on some of the new features:

Virtex Floorplanner: high-end FPGA and ASIC designers want a graphical method, traditionally a floorplanner, to place logic in a device in order to optimize placement for performance. Xilinx introduced the PLD industry's first floorplanner several years ago and now offers one for Virtex FPGAs.

Hierarchical browsing in timing analyzer: Xilinx provides a sophisticated and comprehensive timing analyzer for performance analysis of a design. We have improved this data's organization and display through the use of a Microsoft Explorer-like interface.

STAMP model generation: Chip-to-chip timing analysis has become a critical consideration for customers doing high performance design. Xilinx FPGAs and CPLDs are now used in very high-speed applications where board-level static timing analysis is a required step in the verification flow. The Xilinx implementation tools now output device STAMP models which can be used by Mentor's Tau and Viewlogic's BLAST static timing analysis tools.

CPLD ChipViewer: CPLD designer productivity has been improved through a graphical method for pin assignment as well as viewing the resources used by a design inside the targeted CPLD. Familiar to FPGA designers, it is now available for CPLDs.

Virtex Synopsys LMG SmartModel support: SmartModels integrate smoothly with Xilinx FPGA design tools for complete verification of a complex programmable device in its target system. The SmartCircuit technology develops the models and offers fast simulation performance, a short debug loop (simulate—modify design—re-simulate), and reduced simulation start-up times and netlist extraction delays when compared to traditional gate-level modeling techniques.

PROBE: the use of a logic analyzer to interrogate a specific signal path inside of a complex FPGA has been a complicated task. PROBE allows the user to easily connect an internal signal to a device output pin using a simple graphical tool.

HTML based online manuals: designers no longer need to install hundreds of megabytes of software documentation on their computer in order to get their answers quickly from software documentation. Xilinx has converted thousands of pages to HTML format so documents can be very quickly browsed via the Internet.

Which new device families will version 2.1i development systems support?

The version 2.1i development systems have expanded support to include the new XC9500XV family and package and speed file enhancements to the Virtex family.

The 9500XV family is the industry's first 2.5-volt Flash-based CPLD. This family was first made available to Xilinx customers through a v1.5i service pack, delivered over the Internet, and is now being shipped to all customers in the v2.1i product.

How much do the v2.1i development systems cost?

Foundation Series software is available in configurations priced from $95 to $4995, and Alliance Series software from $95 to $5995.

Why is the product named v2.1i?

2 –indicates a major software release, featuring significant algorithmic improvements. The dramatic runtime and performance improvements that are realized through the use of these algorithms are described in detail below.

.1 –indicates the maturity of the tools. Xilinx always improves the quality of the software that its customers receive from one release to the next. As such, Xilinx has done extensive internal testing on the 2.0 release to ensure that the customer shipped release and meets higher quality standards than those of the 1.5i release.

i –for Internet and continues our Silicon Xpresso initiative, indicating the information rich environment that our customers has access to. This release leverages the productivity enhancements made available to our customers using the Internet

Are there any new cores included as part of this release?

Yes. With each new release of Xilinx development systems new Cores are added to our already robust offering of verified cores. To learn more about the new Cores in this release, please visit the Xilinx IP Center from the Xilinx home page: www.xilinx.com

How does v2.1i performance compare to the previous release, v1.5i?

Compile times for Virtex devices are twice as fast as the previous release and clock frequencies are 30 percent faster due to the introduction of new implementation algorithms for Virtex. Along with base technology improvements in the mainstream development systems, compilation times for Spartan, XC4kX and older programmable logic families were accelerated.

Did Xilinx improve its Alliance EDA Partner integration for system level verification?

Yes, through addition of: Board level static timing analysis (support by Mentor Tau and Viewlogic BLAST); Synopsys LMG SmartModel support (board level behavioral simulation); and improved VITAL and Verilog support (Xilinx Simprim/Unisim).

Is Xilinx v2.1i Year 2000 compliant?

Yes. See our Year 2000 Readiness Statement at www.xilinx.com/company/y2k.htm

XILINX ALLIANCE and FOUNDATION SERIES FEATURES

Design environment for ➔	Schematic & Synthesis		Schematic & ABEL		Schematic & Synthesis	
Features Included	**ALI-BAS**	**ALI-STD**	**FND-BAS**	**FND-STD**	**FND-BSX**	**FND-EXP**
EDA Libraries and Interface for Cadence, Mentor, Synopsys, and Viewlogic	✓	✓				
Turns Engine (Workstation Only)	✓	✓				
Synthesis Constraint Editor, Timing Analyzer (TimeTracker™), and Schematic Viewer (VISTA™)						✓
HDL Synthesis Tools (VHDL & Verilog)					✓	✓
Xilinx ABEL Synthesis			✓	✓	✓	✓
HDL Design Tools: *HDL Wizard, Context Sensitive Language Editor, Graphical State Editor and Language Assistant*			✓	✓	✓	✓
Schematic Editor			✓	✓	✓	✓
Simulator (Functional & Timing)			✓	✓	✓	✓
HDL Simulation Libraries (UniSim and Simprim)	✓	✓	✓	✓	✓	✓
Implementation Tools: *Design Manager, Flow Engine, Timing Analyzer, Hardware Debugger, Core Generator, JTAG Programmer, PROM File Formatter, Graphical Constraints Editor, Graphical Floorplanner*	✓	✓	✓	✓	✓	✓
Internet Team Design Ready	✓	✓				
EDIF, VHDL (VITAL), and Verilog back annotation	✓	✓	✓	✓	✓	✓
LogiBLOX Module Generator	✓	✓	✓	✓	✓	✓
Xilinx Core Generator	✓	✓	✓	✓	✓	✓
CPLD Devices (XC9500 / XL / XV)	✓	✓	✓	✓	✓	✓
FPGA (Low Density/High Volume Devices): *XC4000E/X (Up to XC4013E/X)* *Spartan & SpartanXL (All)* *XC3x00A/L (All)* *XC5200 (Up to XC5210)* *Virtex (V50 only)*	✓	✓	✓	✓	✓	✓
FPGA (Unlimited Device Support): *Virtex (Up to V1000); XC4000E/X - (All); Spartan & SpartanXL (All);* *XC3x00A/L (All); XC5200 (All)*		✓		✓		✓