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FOR IMMEDIATE RELEASE

XILINX ANNOUNCES SUPPORT FOR TWO-MILLION-GATE FPGAS

Xilinx Alliance Series software delivers industry's fastest compile times and first Internet Team Design methodology

SAN JOSE, Calif., May 17, 1999—Xilinx Inc., (NASDAQ:XLNX) today announced its new Alliance Series version 2.1i software. Version 2.1i software delivers 50 percent reduction in compile times over the previous version, v1.5i software. This continues the trend that Xilinx has established during the last few years of reducing compile times for a given design size by 50 percent with each release. This new version also delivers advanced methodologies that support the design of the industry's first two-million-gate Virtex FPGAs, with these devices available later this year. Demonstrations of Alliance Series version 2.1i software will be given at the Design Automation Conference in Xilinx booth #2532.

"The designs that are being implemented in programmable logic today are more complex and are representing the most strategic aspects of our customers systems, said Rich Sevcik, Xilinx senior vice president of software, cores and support. "Our Internet Team Design (ITD) capabilities allow customers to implement designs and share IP across design teams and geographies, which is paramount in designing systems-based programmable logic."

Along with the runtime improvements and increased clock speeds, this release includes the new Xilinx Internet Team Design (ITD) methodology allowing teams of designers around the world to collaborate on multi-million gate designs via the Internet. Other productivity enhancing features of the v2.1i release are the new CORE Generator interface, improved floorplanning, data sheet-style timing reports, and a hierarchical browser for doing comprehensive post-layout timing analysis.

Two-Million-Gate Support

The next generation of place and route capability from Xilinx results in a significant reduction in placement times for Virtex-based architectures. This dramatically increases designer productivity as it enables many design iterations each day—even when designing with the two million plus system gate Virtex devices.

–more–

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FOR IMMEDIATE RELEASE

XILINX AND MENTOR GRAPHICS ANNOUNCE STAMP SUPPORT FOR SYSTEM-LEVEL VERIFICATION

SAN JOSE, Calif., May 17, 1999—Xilinx Inc., (NASDAQ:XLNX) and Mentor Graphics Corporation, (NASDAQ:MENT) today jointly announced support for Stamp file format, bringing easy-to-use board-level timing verification capability to mainstream design engineers.

The industry-standard, Stamp file format output is generated by the new Xilinx Alliance Series software version 2.1i. The Mentor Graphics Tau™ 2.1 board timing verification software reads Stamp models. These models specify pin-to-pin timing delay and constraint information for components. Xilinx is the first PLD supplier to output the Stamp file format from its implementation software.

"Combined with our world class implementation tools, our CORE Generator, and the superior Virtex FPGAs, Xilinx has the complete solution for system-level integration," said Rich Sevcik, senior vice president software, cores, and support.

The Stamp format simplifies the design flow by using a single industry standard rather than multiple standards like SDF, structural Verilog and a technology library. Users no longer need to manage a library of standards and file formats. Additionally users no longer need to create component models from scratch—an arduous and time-consuming process. Because the Tau product can read Stamp models, board design engineers now have an automated solution for FPGA model generation. The close link between Xilinx and the Tau product is particularly important given the many revisions an FPGA goes through, and the need to have the most up-to-date timing information for accurate timing verification.

"This new capability from Xilinx will significantly shorten the time required to verify board timing," said Henry Potts, vice president and general manager of the Board Design Solutions Division at Mentor Graphics. "Combined with Tau, Xilinx Stamp support gives board designers the timing verification solution they need to deliver high-performance, reliable boards that work first time, on time."

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FOR IMMEDIATE RELEASE

XILINX FOUNDATION SERIES SOFTWARE ENABLES DROP-IN 64 BIT/66 MHZ PCI DESIGN

Version 2.1i fast compile times, seamless integration of FPGA Express,
and the Xilinx Core Generator tool simplifies high-performance design

SAN JOSE, Calif., May 17, 1999—Xilinx Inc., (NASDAQ:XLNX) today announced that version 2.1i of the Foundation Series software delivers the industry's fastest compilation times while improving typical system clock speeds. The Foundation Series software has also been improved by embedding the Synopsys' FPGA Express v3.2 and the popular Xilinx CORE Generator tools. The seamless integration of this suite of design tools into the software's intuitive project management system enables drop-in 64 bit, 66 MHz PCI design. Demonstrations of Foundation Series version 2.1i software will be available at the Design Automation Conference in Xilinx booth #2532.

Runtime improvements as a corporate focus

"Two years ago, our designers were excited with place-and-route times on the order of 10,000 gates per hour," said Rich Sevcik, senior vice president of software, cores, and support. "Today with Virtex, they are implementing 100,000 system gates in less than one minute. These advancements, coupled with the ability to drop-in high-level system functions, are driving the phenomenal increase in the programmable content of many digital systems**."**

Through an extensive Xilinx customer benchmarking program, Xilinx tracks a consistent trend over the last several years of increasing average clock speed or performance, while also halving the design compilation time with each successive release. These improvements significantly contribute to the ability to iterate a Xilinx design in minutes, which increases the time-to-market advantages of programmable logic.

Advanced synthesis capabilities

Today, many designers are using hardware description languages (HDLs) to simplify their design flows. Xilinx has worked closely with OEM partner Synopsys to improve the inference and optimization capabilities of the FPGA Express synthesis tool for high-performance results through push-button flows for HDL designs. Foundation Series v2.1i products embed the new FPGA Express

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FOR IMMEDIATE RELEASE

XILINX AND PARTNERS TO DEMONSTRATE INTERNET-BASED DESIGN AT DAC

Remote teams collaborate on complex designs using Internet Team Design (ITD) technology

SAN JOSE, Calif., May 17, 1999—Continuing with its Silicon Xpresso initiative, Xilinx, Inc., (NASDAQ:XLNX) today announced its Alliance partners will show their support for its Internet Team Design (ITD) technology with real-time demonstrations at the Design Automation Conference (DAC) in June.

ITD technology leverages Java language to combine Xilinx design implementation tools and the Internet for remote design teams to work together effectively on today's large, complex FPGA designs. As part of the demonstration, users will access the ITD web site from the Alliance partner booths using a web browser. For the first time, designers will be able to utilize the power of this technology by creating design modules using any entry method at the Alliance Partner booths and sending them over the Internet to the Xilinx booth where results will be compiled and the design completed. Demonstrations will be available at Xilinx booth (#2532), Exemplar booth (#1842), Synopsys booth (#1215) and Synplicity booth (#2032).

Xilinx is the first programmable logic vendor to provide this infrastructure for organizing and coordinating multiple modules, integrating a variety of files, and linking multiple design projects that have been created by design teams and individuals working in different locales. ITD technology differs from other team-based design environments in its platform independence and use of standard web browsers as a design interface, eliminating a learning curve.

The size and use of programmable logic has been expanding rapidly and creating new challenges for design teams. These challenges include large and complex designs, multiple design inputs, from schematic to HDL, and remote locations of the designers. ITD technology addresses these challenges through internet-based communication; multiple input integration (including VHDL, Verilog, schematics and cores); and design coordination through an intelligent Design Control System (DCS).

–more–

“By using the Design Control System in the ITD solution, the project leader can work with a wide variety of engineers and design inputs in various locations,” said Rich Sevcik, Xilinx senior vice president of software, cores and support. “ITD technology provides the means to efficiently and effectively integrate and coordinate the design inputs on an iterative basis. Designers will see how the project leader can use ITD technology and the Internet today to manage large design teams through complex projects for creating next-generation applications.”

Exemplar Logic, a wholly owned subsidiary of Mentor Graphics Corporation, supports Xilinx Virtex FPGAs in its advanced synthesis tool, LeonardoSpectrum. LeonardoSpectrum is a synthesis environment designed to handle the largest and most complex FPGA devices. The gate array market segment, a focus of both Exemplar Logic and Xilinx, demands team-based design and Internet-based tools. “ITD technology meets the challenges of team design,” said Tom Feist, vice president of marketing for Exemplar Logic. "It is a natural extension of LeonardoSpectrum's team design capabilities. Exemplar’s robust support for bottom-up and incremental design, combined with Xilinx ITD communication and design integration capabilities help to create an effective working environment for dispersed design teams.”

"The Internet eases the communications burden for engineering teams collaborating with designers and partners working on the same project from different locations," according to Jay Michlin, vice president and general manager of the FPGA business unit at Synopsys. "This is particularly important for large devices in which teams are already splitting projects among remote sites which use Synopsys' world-class synthesis and verification tools to design each module. The Xilinx introduction of its Internet Team Design technology will allow designers to leverage the Internet to deliver modules around the world, and then complete their design in the chosen location."

Andy Haines, vice president of marketing for Synplicity Inc. is excited to be working with Xilinx on the implementation of the ITD methodology. "Maximizing designer productivity is of prime importance to Synplicity. Xilinx's use of the Internet to join our tools with theirs is an out-of-the-box approach to increasing productivity. This is another example of the close working relationship between

Synplicity and Xilinx, just as is the superior quality of results from our Synplify synthesis tool when targeting the Virtex architecture."

Xilinx is the leading innovator of complete programmable logic solutions, including advanced integrated circuits, software design tools, predefined system functions delivered as cores, and unparalleled field engineering support. Founded in 1984 and headquartered in San Jose, Calif., Xilinx invented the field programmable gate array (FPGA) and commands more than half of the world market for these devices today. Xilinx solutions enable customers to reduce significantly the time required to develop products for the computer, peripheral, telecommunications, networking, industrial control, instrumentation, high-reliability/military, and consumer markets. For more information, visit the Xilinx web site at www.xilinx.com.

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synthesis technology within its design environment. Advances in the synthesis and optimization of a variety of functions, including multiplexors, are yielding results that run twice as fast and occupy 50 percent of the area when compared to the current Foundation Series product. The combined performance and runtime improvements of FPGA Express with Xilinx v2.1i implementation tools deliver the most powerful, ready-to-use HDL development environment in the industry.

In addition to performance and runtime improvements, FPGA Express also delivers new, advanced HDL design capabilities like Integrated Schematic Viewing and Static Timing Analysis (Vista), and TCL-based scripting. These powerful HDL development tools, along with the other value added HDL design tools assist Foundation Series customers in their creation of HDL designs that are optimal for Xilinx programmable logic devices.

Drop-in PCI design

The Foundation Series v2.1i software features seamless integration of the Xilinx CORE Generator tool, which simplifies the use of advanced Intellectual Property (IP) or cores. The improved design flow links the schematic capture and HDL editor tools directly to the CORE Generator tool which allows designers to implement core functions with guaranteed performance. The tool generates custom, optimized design files, based on user parameters, with predictable timing and VHDL or Verilog simulation models.

In addition, the Foundation Series tools enable customers to create a 64-bit, 66 MHz PCI interface in a Virtex device or a 32-bit/33 MHz PCI interface in a SpartanXL device—both customizable and fully compliant with guaranteed timing. The Virtex-based PCI solution is the industry's first general-purpose 64-bit/66 MHz PCI solution. The Spartan-based solution enables designers to complete a PCI bridge at a component cost below $5.00.

Other ease-of-use capabilities in the Foundation Series new version include advanced error and timing navigation, design wizards, intuitive GUIs, and powerful synthesis scripting capabilities.

Pricing, platform, and availability

The Foundation Series 2.1i software supports the design of all Xilinx programmable logic device families, including Spartan/XL, Virtex, XC4000X, XC4000XV, XC3100A/L, and XC5200 FPGAs, plus the XC9000 series of flash based CPLDs. Xilinx development systems are available for PC and workstation platforms and operating systems, including PCs running Windows95 and Windows NT; Chinese, Korean, and Japanese Windows; and workstations running Solaris and HP-UX. The

Xilinx v2.1i Software Backgrounder

Alliance Series Software / Foundation Series Software

Introduction

Xilinx delivers the most powerful programmable logic solution in the industry. The combination of Xilinx software and cores, leading edge Xilinx FPGA and CPLD device architectures, and comprehensive support services make Xilinx the preferred choice of electronic designers worldwide.

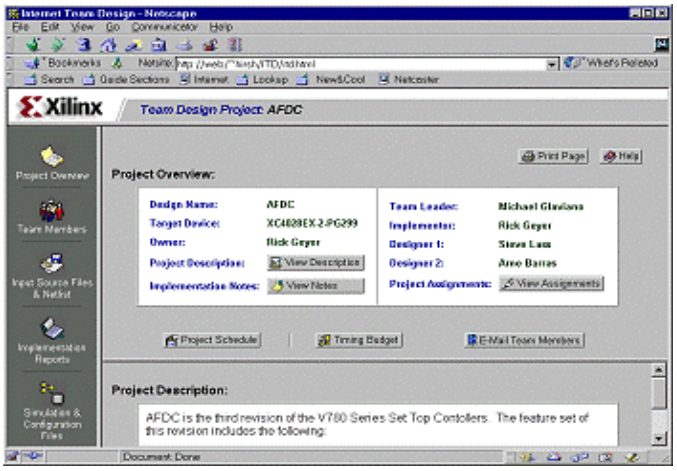
Configurations

Version 2.1i consists of two flagship products:

- Alliance Series Software - The Alliance Series is engineered to plug and play with a digital designer's existing design flow. This combination of advanced feature sets delivers high performance results within a customizable design environment.
- Foundation Series Software - The Foundation Series Software is a complete, ready-to-use design environment that integrates schematic, synthesis, verification, and implementation tools into an intuitive, yet highly advanced design solution.

Internet Team Design

Version 2.1i enables teams of designers to collaborate on a design using the internet as the communications backbone. Designers will be able to use their Netscape™ or Microsoft™ browser to coordinate a design project from across the aisle or across the world.



Xilinx Extends its Cores Leadership

Designers that need PCI, DSP, memory blocks, soft cores from Xilinx AllianceCORE Partners, or other intellectual property in their designs will reap significant productivity benefits via the newly enhanced CORE Generator, which is integrated with the Alliance and Foundation Series software. Using the Core Generator, designers can take advantage of the world's 1st 64 bit/66 MHz Real PCI Core.

The Real-PCI™ 64/66

Industry's First 2 Million Gate FPGA

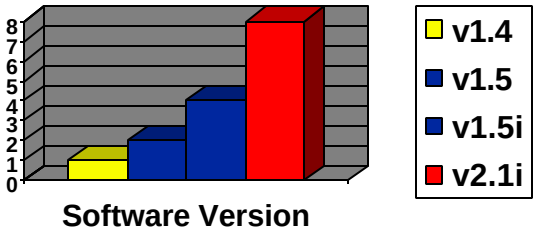
The Virtex family redefines the future of programmable logic by delivering FPGAs that break density and performance barriers while offering unprecedented system level integration. Plus, Xilinx offers an extensive library of cores which allows designers to create very complex, high speed designs with guaranteed results. There has never been an easier or faster way to get a digital design to market.

VIRTEX™

Industry's FASTEST Runtimes

The Implementation Tools that are included in the Alliance and Foundation tools are the key to achieving industry's fastest compile times. Xilinx has doubled the speed of its Place and Route tools in each of the last 4 releases. Fast compile times translate to more turns per day and greater productivity.

Compiler Speed Improvements



Support

Xilinx support resources serve as an extension of a company's design team. Xilinx delivers comprehensive support services including:

SUPPORT.XILINX.COM

- support.xilinx.com: a designer-centric web site that is available 24 hours a day, 7 days a week
- Worldwide phone-based support during working hours
- XPERTS Certified Third Party Consultants Program
- Customer Education Services
- The IP Center: a web-based resource for Cores & IP
- Local Field Application Engineers

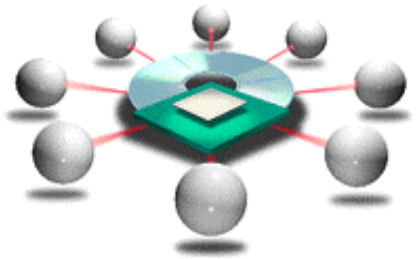
Summary

The 2.1i versions of the Alliance and Foundation Series software enable designers to deliver the world's highest performing digital designs on time and to spec. Version 2.1i delivers extremely fast compile times and super fast clock speeds. In addition, Xilinx's superior Cores strategy will significantly speed up a project's time-to-market. *The 2.1i release represents the most productive, most effective programmable logic design environment available today.*

Xilinx Programmable Logic Design Solutions

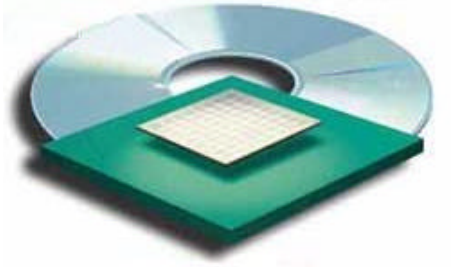
Version 2.1i

ALLIANCE Series Software



Designing the Industry's First 2 Million Gate FPGA

FOUNDATION Series Software



Drop-In 64 Bit / 66 MHz PCI Design

XILINX®

Frequently asked Questions and Answers

for Xilinx version 2.1 Software

What product configurations are available for the v2.1i development systems?

Xilinx offers its development systems in two series of products to match customer design requirements – The Alliance and Foundation Series software.

The Xilinx Alliance Series software is a state-of-the-art programmable logic development system that features advanced integration into the tool suites from Alliance Partners such as Exemplar, Mentor, Synopsys, and Synplicity.

The Foundation Series software provides a ready-to-use programmable logic design environment in a number of cost effective configurations. This environment includes Schematic and HDL design entry tools, ABEL, VHDL, and Verilog synthesis using Synposys FPGA Express, Xilinx 2.1i implementation tools, and a robust set of verification capabilities.

Who are the Xilinx Alliance partners?

Xilinx works closely with each of the leading EDA vendors to ensure high quality results when using third-party EDA tools with Xilinx advanced implementation tools. A full list of these partners is available at: www.xilinx.com/programs/alliance/alligen.htm#CAT

When will the v2.1i development systems ship to customers?

The first v2.1i-based product to ship will be the Xilinx Alliance Series product, available in June 1999. Foundation Series shipments will begin in July 1999.

What new features are there in the version 2.1i development systems?

Development efforts for the v2.1 software have been focussed on Internet enabled design capabilities including Internet Team Design (ITD) methods, compile time reductions, improvements to design clock speed, and continuing to improvement in productivity and ease-of-use.

The Xilinx Alliance Series products have a several unique capabilities that were added for the v2.1i release, including support for STAMP models, and Xilinx Internet Team Design capabilities.

The Xilinx Foundation Series is improved through the inclusion of Synopsys FPGA Express v3.2, better design flow automation, and the embedding of the Xilinx CORE Generator tool. Features that are specific to Synopsys® FPGA Express™ 3.2 release include the first production shipment of Vista™, the use of NCF for EDIF and XNF netlist flows, TCL scripting capabilities, and dramatic improvements in quality of result and runtime for designs, which include multipliers.

Some specific features added to the implementation tools—common to both Foundation Series and Alliance Series products—are:

- floorplanner support for the Virtex family
- fast, hierarchical browsing in timing analyzer
- CPLD ChipViewer tool for quick, graphical pin assignment and layout analysis
- FPGA Editor, including the probe capability for fast design debug in the lab
- new and improved constraints editor
- HTML-based documentation for quick browsing
- Synopsys LMG Smartmodel™ support for Virtex FPGAs

Further details on some of the new features:

Virtex Floorplanner: high-end FPGA and ASIC designers want a graphical method, traditionally a floorplanner, to place logic in a device in order to optimize placement for performance. Xilinx introduced the PLD industry's first floorplanner several years ago and now offers one for Virtex FPGAs.

Hierarchical browsing in timing analyzer: Xilinx provides a sophisticated and comprehensive timing analyzer for performance analysis of a design. We have improved this data's organization and display through the use of a Microsoft Explorer-like interface.

STAMP model generation: Chip-to-chip timing analysis has become a critical consideration for customers doing high performance design. Xilinx FPGAs and CPLDs are now used in very high-speed applications where board-level static timing analysis is a required step in the verification flow. The Xilinx implementation tools now output device STAMP models which can be used by Mentor's Tau and Viewlogic's BLAST static timing analysis tools.

CPLD ChipViewer: CPLD designer productivity has been improved through a graphical method for pin assignment as well as viewing the resources used by a design inside the targeted CPLD. Familiar to FPGA designers, it is now available for CPLDs.

Virtex Synopsys LMG SmartModel support: SmartModels integrate smoothly with Xilinx FPGA design tools for complete verification of a complex programmable device in its target system. The SmartCircuit technology develops the models and offers fast simulation performance, a short debug loop (simulate—modify design—re-simulate), and reduced simulation start-up times and netlist extraction delays when compared to traditional gate-level modeling techniques.

PROBE: the use of a logic analyzer to interrogate a specific signal path inside of a complex FPGA has been a complicated task. PROBE allows the user to easily connect an internal signal to a device output pin using a simple graphical tool.

HTML based online manuals: designers no longer need to install hundreds of megabytes of software documentation on their computer in order to get their answers quickly from software documentation. Xilinx has converted thousands of pages to HTML format so documents can be very quickly browsed via the Internet.

Which new device families will version 2.1i development systems support?

The version 2.1i development systems have expanded support to include the new XC9500XV family and package and speed file enhancements to the Virtex family.

The 9500XV family is the industry's first 2.5-volt Flash-based CPLD. This family was first made available to Xilinx customers through a v1.5i service pack, delivered over the Internet, and is now being shipped to all customers in the v2.1i product.

How much do the v2.1i development systems cost?

Foundation Series software is available in configurations priced from $95 to $4995, and Alliance Series software from $95 to $5995.

Why is the product named v2.1i?

2 –indicates a major software release, featuring significant algorithmic improvements. The dramatic runtime and performance improvements that are realized through the use of these algorithms are described in detail below.

.1 –indicates the maturity of the tools. Xilinx always improves the quality of the software that its customers receive from one release to the next. As such, Xilinx has done extensive internal testing on the 2.0 release to ensure that the customer shipped release and meets higher quality standards than those of the 1.5i release.

i –for Internet and continues our Silicon Xpresso initiative, indicating the information rich environment that our customers has access to. This release leverages the productivity enhancements made available to our customers using the Internet

Are there any new cores included as part of this release?

Yes. With each new release of Xilinx development systems new Cores are added to our already robust offering of verified cores. To learn more about the new Cores in this release, please visit the Xilinx IP Center from the Xilinx home page: www.xilinx.com

How does v2.1i performance compare to the previous release, v1.5i?

Compile times for Virtex devices are twice as fast as the previous release and clock frequencies are 30 percent faster due to the introduction of new implementation algorithms for Virtex. Along with base technology improvements in the mainstream development systems, compilation times for Spartan, XC4kX and older programmable logic families were accelerated.

Did Xilinx improve its Alliance EDA Partner integration for system level verification?

Yes, through addition of: Board level static timing analysis (support by Mentor Tau and Viewlogic BLAST); Synopsys LMG SmartModel support (board level behavioral simulation); and improved VITAL and Verilog support (Xilinx Simprim/Unisim).

Is Xilinx v2.1i Year 2000 compliant?

Yes. See our Year 2000 Readiness Statement at www.xilinx.com/company/y2k.htm

XILINX ALLIANCE and FOUNDATION SERIES FEATURES

Design environment for ➔	Schematic & Synthesis		Schematic & ABEL		Schematic & Synthesis	
Features Included	**ALI-BAS**	**ALI-STD**	**FND-BAS**	**FND-STD**	**FND-BSX**	**FND-EXP**
EDA Libraries and Interface for Cadence, Mentor, Synopsys, and Viewlogic	✓	✓				
Turns Engine (Workstation Only)	✓	✓				
Synthesis Constraint Editor, Timing Analyzer (TimeTracker™), and Schematic Viewer (VISTA™)						✓
HDL Synthesis Tools (VHDL & Verilog)					✓	✓
Xilinx ABEL Synthesis			✓	✓	✓	✓
HDL Design Tools: *HDL Wizard, Context Sensitive Language Editor, Graphical State Editor and Language Assistant*			✓	✓	✓	✓
Schematic Editor			✓	✓	✓	✓
Simulator (Functional & Timing)			✓	✓	✓	✓
HDL Simulation Libraries (UniSim and Simprim)	✓	✓	✓	✓	✓	✓
Implementation Tools: *Design Manager, Flow Engine, Timing Analyzer, Hardware Debugger, Core Generator, JTAG Programmer, PROM File Formatter, Graphical Constraints Editor, Graphical Floorplanner*	✓	✓	✓	✓	✓	✓
Internet Team Design Ready	✓	✓				
EDIF, VHDL (VITAL), and Verilog back annotation	✓	✓	✓	✓	✓	✓
LogiBLOX Module Generator	✓	✓	✓	✓	✓	✓
Xilinx Core Generator	✓	✓	✓	✓	✓	✓
CPLD Devices (XC9500 / XL / XV)	✓	✓	✓	✓	✓	✓
FPGA (Low Density/High Volume Devices): *XC4000E/X (Up to XC4013E/X)* *Spartan & SpartanXL (All)* *XC3x00A/L (All)* *XC5200 (Up to XC5210)* *Virtex (V50 only)*	✓	✓	✓	✓	✓	✓
FPGA (Unlimited Device Support): *Virtex (Up to V1000); XC4000E/X - (All); Spartan & SpartanXL (All);* *XC3x00A/L (All); XC5200 (All)*		✓		✓		✓

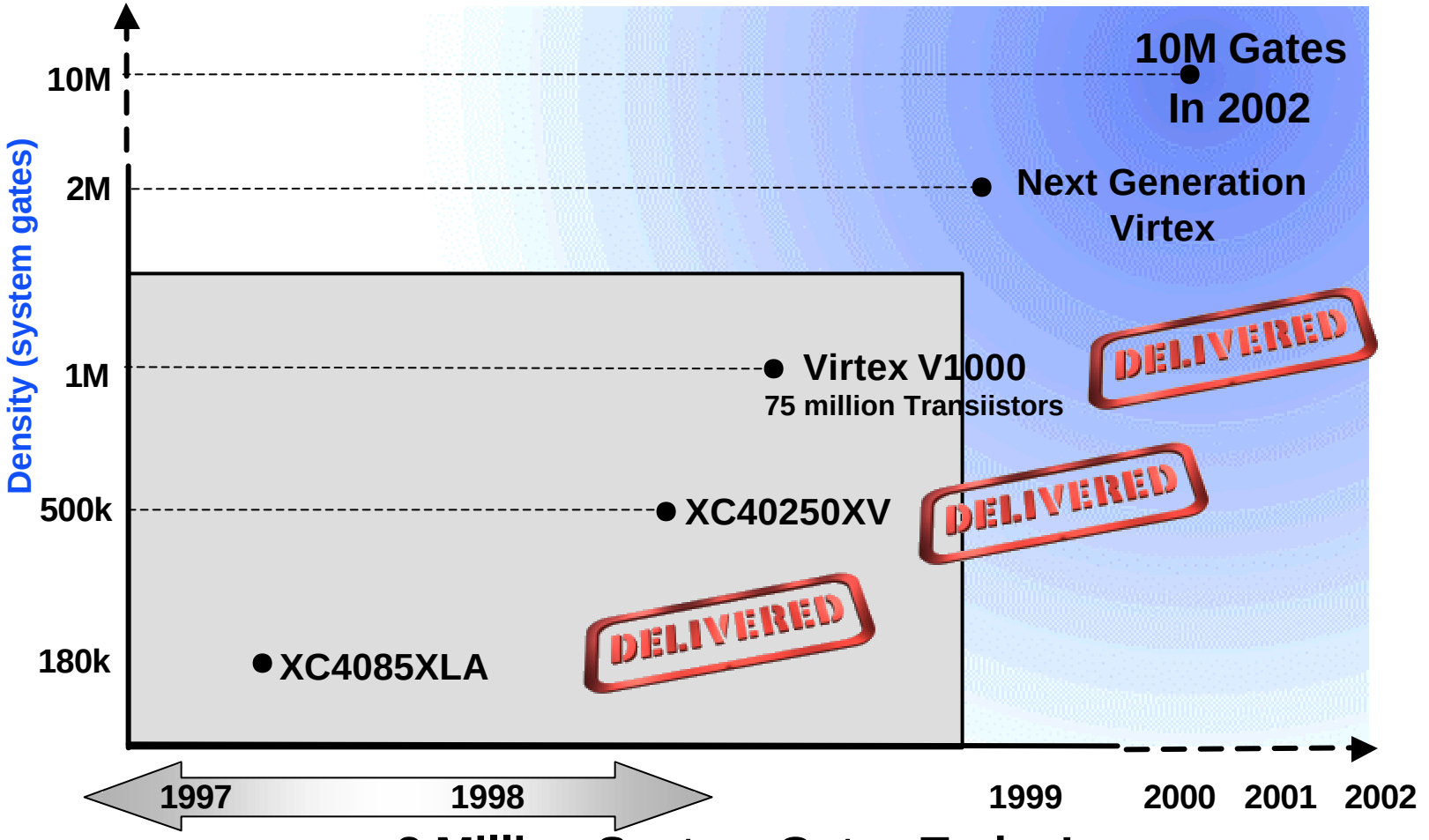
State of the Art Programmable Logic Design

- Industry's fastest compilation times
- Industry's highest performance
- Industry's best support for High-Level design flows
  - HDL design
  - Design re-use / Cores
  - Robust functional and timing verification
  - Internet enabled design

- Support for the industry's largest FPGAs
- Products configured to meet your design needs

XILINX®

Density Leadership



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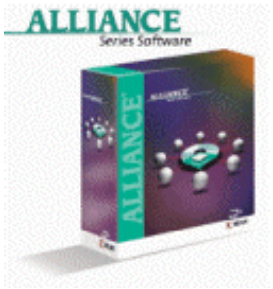
Software Leadership



DELIVERED

v1.5i **Ease Of Use**

- ✓ Push Button Design
- ✓ Minimum Delay Reporting
- ✓ Voltage/Temperature Prorating
- ✓ Floorplanning

DELIVERED

v2.1i **Internet Enabled Software**

- ✓ Internet Team Design
- ✓ 2 Million Gate support
- ✓ 100K Gates < 1 minute
- ✓ Embedded Core Generator
- ✓ Drop-In 64 bit / 66 MHz PCI

Xpresso

1998 1999

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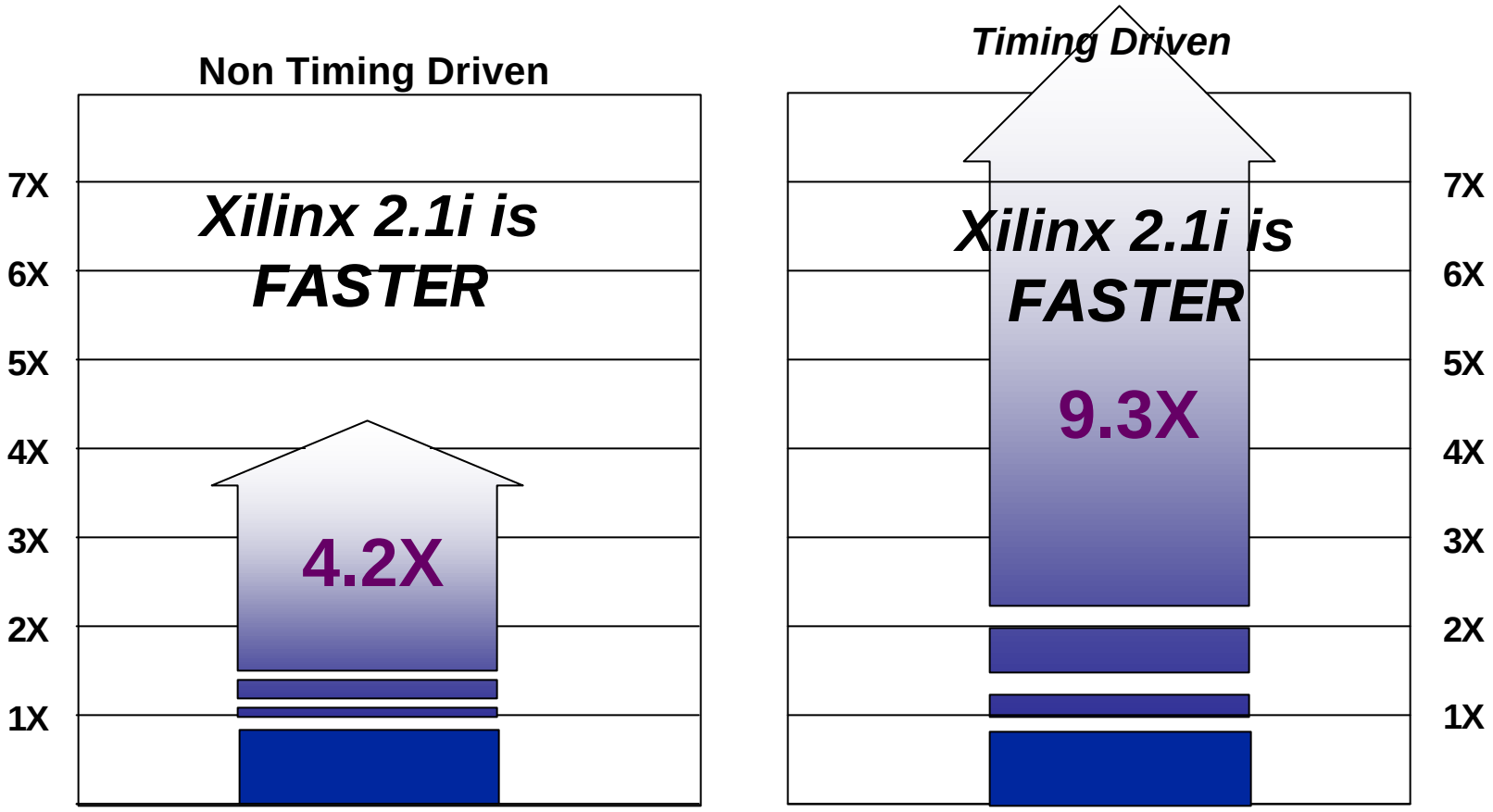
Benchmark Results

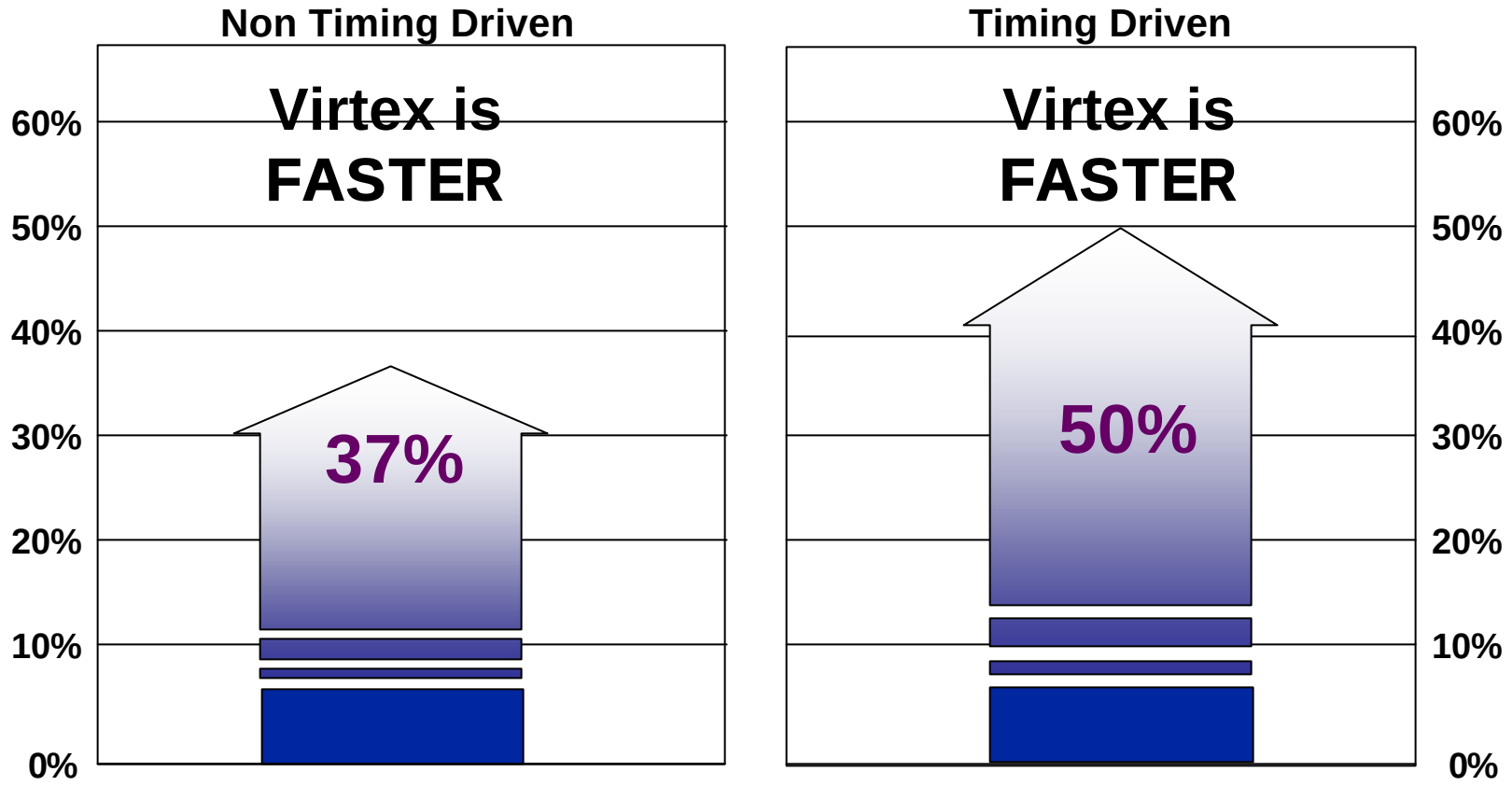
Virtex vs. 10KE Compilation Time



- Benchmarks are comparing Virtex -6 with 10KE-1 using Alliance version 2.1i vs. MAX+PLUS2 9.1
- Design suite consists of 22 HDL customer designs ranging from XCV50-XCV600

Benchmark Results

Virtex vs. 10KE Performance



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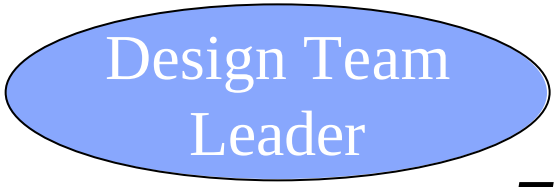
VIRTEX

XILINX®

Internet Team Design

Solves 21st Century Design Challenges

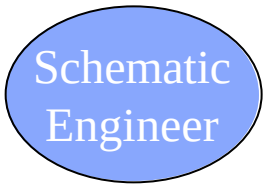


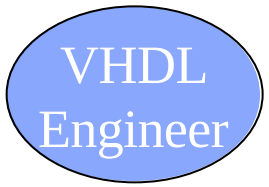
The Problem

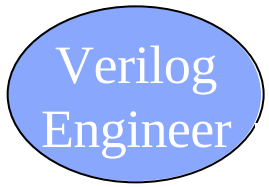
- Million+ Gate Designs
- Variety of Flows
- Remote Location of Designers
- Design Revision Management

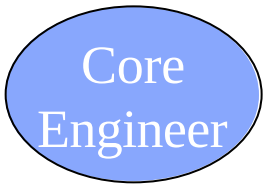
The Solution

- Communication
- Coordination
- Integration









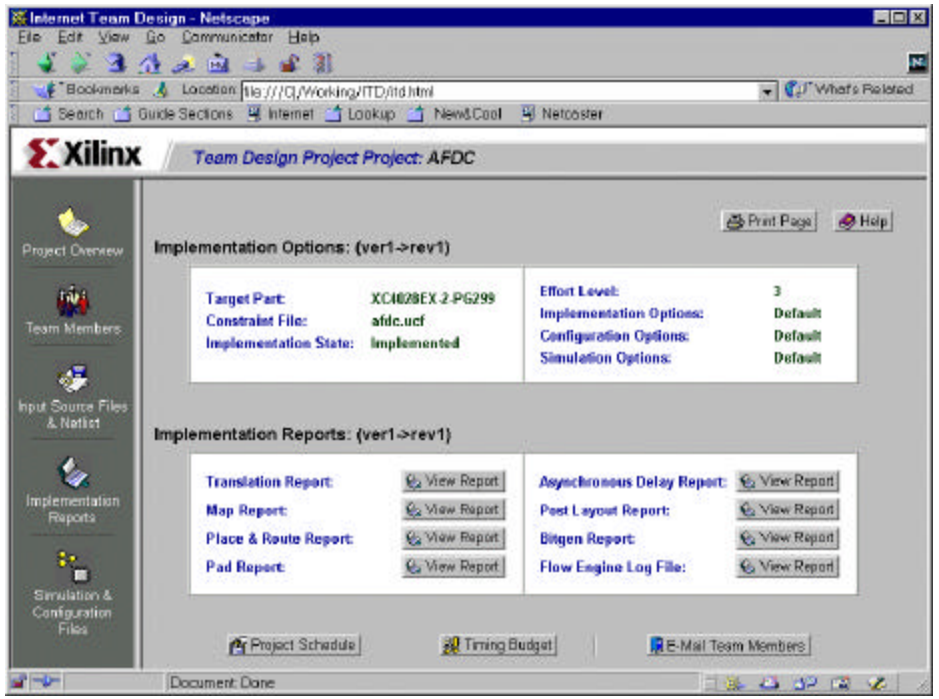
XILINX®

Internet Team Design
Product Description

A web-based facility to coordinate and manage team-based design projects

Key features include:

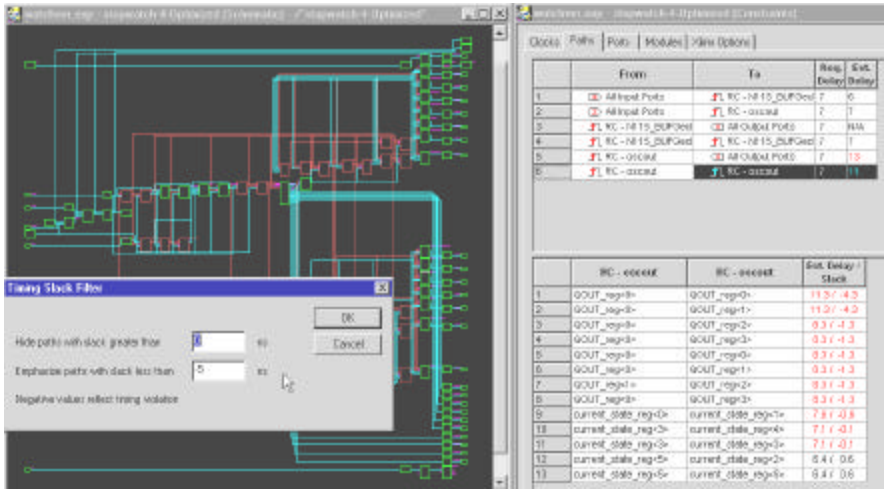
- Facilitates project schedule, assignments and communication among team members
- Coordination of input source and netlist files from multiple designers
- Provides access to implementation reports, timing simulation and configuration files



XILINX®

Synopsys
FPGA Express™ 3.2

- Push-Button HDL Performance:
  - Advanced synthesis delivers faster clock speeds, and more efficient utilization



- Powerful HDL design:
  - TCL scripting enables ASIC - style design flow
  - Advanced Analysis features simplify design debugging:
    - Integrated Schematic Viewing and Static Timing Analysis (VISTA™)
    - Consistent signal naming

XILINX®

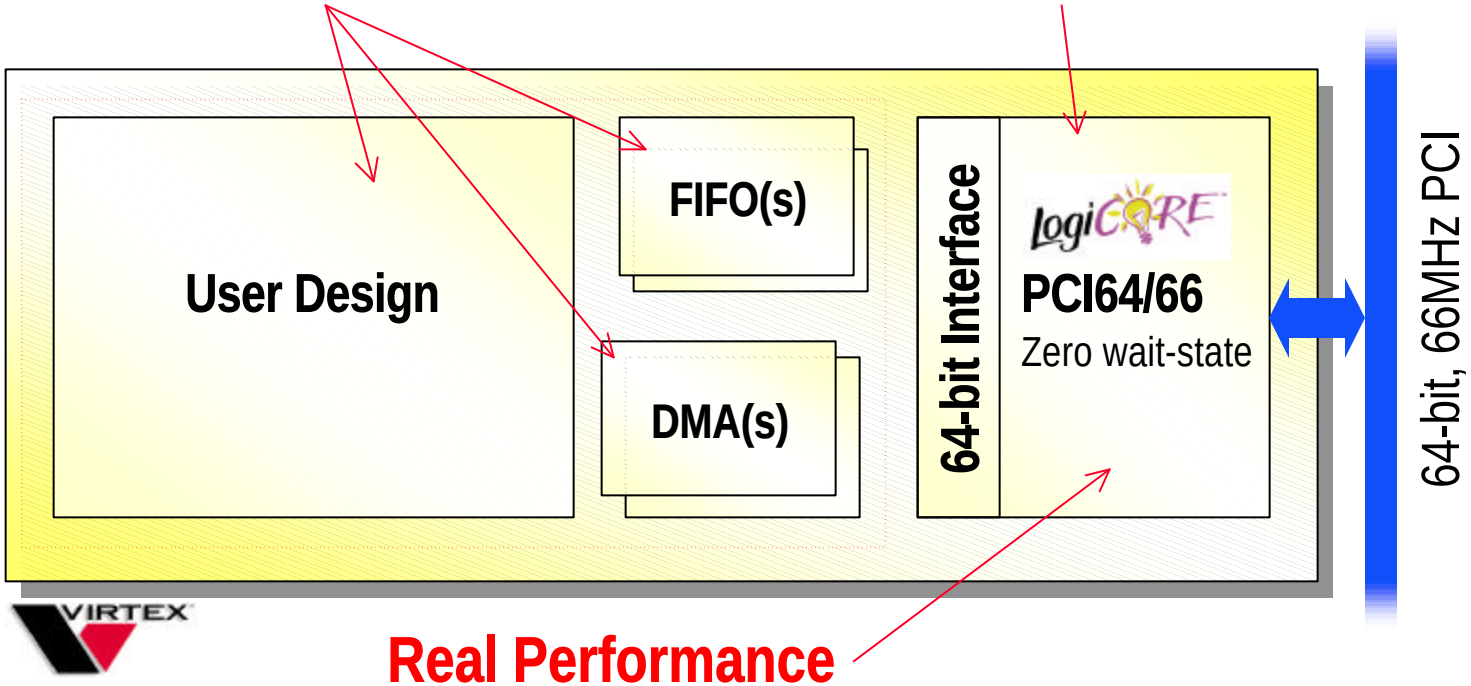
The Real 64/66 PCI

Real Flexibility

- Uses standard Virtex FPGA
- Back-end de-coupled from core

Real Compliance

- PCI v2.2 Initiator and Target
- Guaranteed timing



Real Performance

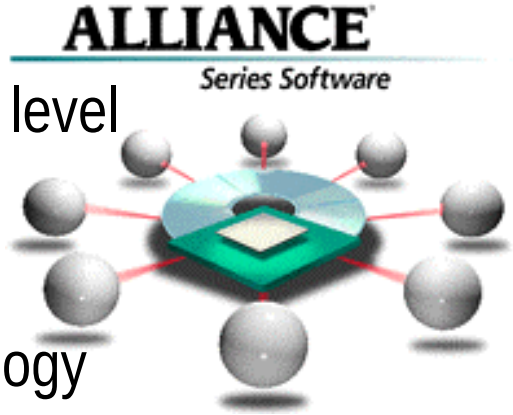
- Compliant zero wait-state at 66MHz
- Full 64-bit data path

XILINX®

Xilinx Alliance Series

Programmable Logic Design Tools Integrated Into Your EDA Environment

- Robust support for the complexities of multi-million gate FPGA design
  - High performance synthesis
  - Advanced design analysis through board level verification
    - STAMP and LMG models
- Industry's first Internet Team Design methodology
- Productivity enhancements speed system level design
  - Dramatic compile time improvements
  - Extensive IP
  - Design timing and layout analysis tools



XILINX®

Xilinx Foundation Series

A Complete, Ready to Use Programmable Logic Design Environment

- Easy to use, mixed-level design environment
  - Industry's fastest compilation times
  - Embedded core generation tool
  - Industry's most comprehensive on-line support
- Powerful, mixed-language synthesis from Synopsys®
- Drop-In PCI design
  - 64 bit / 66 MHz Virtex "Real PCI"
  - 32 bit / 33 MHz SpartanXL PCI

Foundation Series software will be available this summer with pricing starting at $95. Evaluation software is also available for qualified users at no cost.

Xilinx is the leading innovator of complete programmable logic solutions, including advanced integrated circuits, software design tools, predefined system functions delivered as cores, and unparalleled field engineering support. Founded in 1984 and headquarters in San Jose, Calif., Xilinx invented field programmable gate arrays (FPGA) and commands more than half of the world market for these devices today. Xilinx solutions enable customers to significantly reduce the time required to develop products for the computer, peripheral, telecommunication, networking, industrial control, instrumentation, high-reliability/military, and consumer markets. For more information, visit the Xilinx web site at www.xilinx.com.

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"Board timing verification is a very important step in our design process and we use Tau for this purpose. Also, the timing critical portion of our designs often contain Xilinx FPGAs," said Roger Yang, verification engineer at Cisco Systems. "For this reason, we requested Xilinx to provide pin-to-pin timing information for their FPGAs. The new Stamp model generation capability from Xilinx with both maximum and minimum delay data will greatly simplify the process of verifying FPGA timing as part of a board."

In addition to solving the modeling problem, Tau 2.1 software offers state-of-the-art analysis capabilities. The Tau product uses symbolic timing analysis technology to provide worst-case results in one pass and without false violations.

Symbolic analysis reasons over the functional information in component models to automatically eliminate the reporting of false timing violations. In addition, through its delay correlation capability, symbolic analysis accounts for the tracking of delay within components and correctly handles the "common ambiguity" problem. Tau 2.1 software performs clock tree analysis and computes the skew and phase shift between clocks, taking component and interconnect delay into account.

The SelectI/Os within the Virtex FPGAs enable system designers to interface with a variety of business standards for systems interfacing, general-purpose logic, high-speed SDRAM, and high-speed backplane driver applications, like LVTTL, LVCMOS2, PCI33, PCI66, GTL/GTL+, SSTL, HSTL, and CTT. Stamp models provide a methodology to accurately analyze systems on a board in a language that is widely industry-accepted.

About Mentor Graphics

Mentor Graphics is a world leader in electronic hardware and software design solutions, providing products and consulting services for the world’s largest electronic and semiconductor companies. Established in 1981, the company reported revenues over the last 12 months of $490 million and employs approximately 2,600 people worldwide. Company headquarters are located at 8005 SW Boeckman Road, Wilsonville, Oregon 97070-7777. World Wide Web site: http://www.mentor.com.

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"As device densities reach two-million gates, we remain focused on decreasing compile times," said Sevcik. “At the push of a button, designers can now compile the 100,000 system gate Virtex device in less than one minute. And, given the broad suite of cores supporting Virtex FPGAs today, high-level systems functions including the a 64 bit/66 MHz PCI interface can be implemented in less than 20 minutes."

Through close collaboration with our Alliance EDA partners, synthesis is now optimized for Virtex FPGAs. The ability to infer within synthesis the architectural features such as delay locked loops (DLL) and block RAM provides a more simplified design entry method while improving utilization. This feature coupled with fast compile times enables the productivity necessary to accomplish multiple design turns per day to meet the challenge of decreasing time to market.

Proper board-level verification becomes critical when designing systems with multi-million gate high-performance Virtex parts. Version 2.1i software delivers effective integration into board-level static timing analysis tools—a requirement for these types of designs. Xilinx now provides STAMP models with both minimum and maximum delay timing information for use with Mentor and Viewlogic board-level static timing. For system-level simulation, Synopsys supports Xilinx with its Logic Modeling SmartModels family.

Pioneering Internet Team Design (ITD) methods

Continuing in the Silicon Xpresso initiative and leveraging the current functionality of the Internet, Xilinx has enabled ITD capabilities within this version of Alliance Series software. The ITD tool is an innovative new way to meet the challenges of building complex, mega-gate designs by allowing teams of designers to build high-density programmable logic designs over the Internet. This add-on product will be available for purchase over the Web.

As Xilinx device densities approach two million system gates and beyond, designers must coordinate multiple design modules from others in remote locations. The ITD tools use the Internet to deliver improved communication between all members of the design team; to coordinate the different design source files; and to expertly integrate different design flows seen in today's typical FPGA design.

The ITD method creates a designer website that resides on the users' internal network. This website is a forms-based Web page where designers log-on and submit their design files to the project using their chosen Internet browser. Once submitted, the files are merged into a design project using ITD's Design Control System (DCS). The DCS behaves as a Web-based revision management system

that insures that the various iterations of a design's modules are properly linked into the top-level design. Using the ITD tool, the design team leader can easily integrate the design modules and place-and-route the design using the standard Xilinx implementation tools included within the Xilinx Alliance Series software. Once the design is placed and routed, detailed reports are issued to the ITD website for review by the design team. In this way, the team can brainstorm and collaborate on the creation of any additional iterations.

About Alliance Series software

The Alliance Series 2.1i software provides architecture-specific device support for all Xilinx product families, including Spartan/XL, Virtex, XC4000X, XC4000XV, XC3100A/L, and XC5200 FPGAs, plus XC9000 CPLDs. The new software will be available in June for popular PC and workstation platforms and operating systems such as Windows95 and Windows NT; Chinese, Korean, and Japanese Windows; Solaris and HP-UX. The new Alliance Series software pricing starts at $95. Evaluation software is also available for qualified users.

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