Product Backgrounder
The XC9500 CPLD Family

Introduction

The XC9500 family is the third generation of CPLD products from Xilinx. It is targeted for system manufacturers who require the most complete in-system programming, test, and manufacturing capability to support the entire product life cycle. From initial prototyping, to system integration, manufacturing, and field upgrade, the XC9500 product provides a total support solution with fully integrated in-system operations using a standard IEEE 1149.1 boundary scan (JTAG). The XC9500 family also provides superior pin-locking capability necessary for unexpected changes during design iterations and field upgrades. By using FastFLASH technology, a revolutionary 5 V flash technology optimized for high performance CPLDs, the XC9500 provides a leadership endurance of 10,000 program/erase cycles. This allows the XC9500 devices to be used in applications requiring frequent field upgrades and reconfigurations.

In addition, the XC9500 family provides both performance and density by offering leading pin-to-pin propagation delays as fast as five ns and nine devices ranging in density from 800 to over 12,000 gates.

Product Life Cycle Support

The in-system programming capability can support all stages of the product life cycle. Unlike other competing products, the XC9500 device provides in-system programming capability throughout the full commercial operating range. This simplifies the programming requirements and allows more robust field upgrade operations. In addition to in-system programming, other product requirements are needed to support each of the product life cycle stages.

Prototyping

During initial prototyping, a printed circuit board (PCB) is built to accommodate the CPLD's assigned pinouts. A blank device is soldered on the PCB, and a pattern is programmed into the device. During this time, the device may be reprogrammed many times using the same pinout. If the pinout cannot be locked by the architecture, an expensive and time-consuming re-layout of the PCB must be done. A device may be reprogrammed 10 or more times per day during the prototyping stage. If the entire prototyping stage lasts several weeks, the device may be reprogrammed hundreds of times. By providing industry-leading pin-locking capability and a guaranteed endurance of 10,000 program/erase cycles, the XC9500 fully supports the prototyping stage.

System Integration

When individual subsystems are operational, the entire system is assembled for overall testing and optimization. During system integration, the entire system is tested and debugged. All important logic states should be easily accessible, and internal logic implementations within each CPLD should be capable of being checked. When multiple CPLD designs are used within a system, the ability to track pattern revision becomes an issue. Each XC9500 device supports the IEEE 1149.1 INTEST and USERCODE instructions, which are used to access and debug user logic, and track pattern revisions, respectively. In addition, superior pin-locking and high endurance provides design iterations during system debug.

Manufacturing

Once the development is completed, the system design is transferred to the manufacturing and test teams to put into production. Test programs must developed to fully test the operation of the board and to program the CPLDs. Each XC9500 device may be programmed using the IEEE 1149.1 standard interface, which simplifies the generation of the test and programming vectors. The HIGHZ instruction allows a simple mechanism to float device outputs to allow a easier test flow for "bed of nails" board testing. In addition, the IDCODE and USERCODE

instructions provide electronic signatures for automatic inventory control and pattern revision tracking. By providing the capability to program all XC9500 devices concurrently within the system, the programming overhead during board test is minimized.

Field Upgrades

A system shipped to customers may need to be upgraded in the future. Design changes in the field can occur from fixing bugs, adapting to changing standards, or adding new capability. Systems with remote field upgrade capability have built-in circuitry to reprogram parts of the system internally, by using a microprocessor or other means to program a new pattern into the CPLD. The XC9500 devices support field upgrade capability by providing pin-locking capability and high endurance to accommodate the changes.

Pin-Locking Capability

The XC9500 architecture provides industry-leading pin-locking capability by incorporating the three neceesary elements.

1) 100 percent interconnect of all pins and function block outputs to function block inputs with the FastCONNECT™ switch matrix;
2) wide function block fan-in with 36 total inputs;
3) flexible product term allocation capability whereby additional product terms may be added to any macrocell without affecting adjacent macrocells.

The FastCONNECT switch matrix ensures that the path between any input or function block output to another function block is not blocked by existing routing constraints. (See Figure 1.) There is no need to require the software to re-assign pins in order to free up necessary routing connections.

By providing wide function block fan-in, additional signals may be routed into a function block when needed. (See Figure 2.) This increases the chance that a design change requiring additional signals can be made to each function block.

Finally, the XC9500 architecture allows logic to be optimally allocated as needed to each macrocell within the block. In current architectures that lack this capability, macrocells next to full macrocells may not be able to accommodate new logic changes. This in turn causes their output pins to become reassigned unexpectedly. By eliminating adjacency restrictions, the XC9500 helps to maintain a stable pinout assignment. The macrocell is shown in Figure 3.

FastFLASH™ Technology

FastFLASH technology is the first five volt flash technology for CPLDs. The proprietary 0.6 micron double-poly, double-metal flash process was jointly developed by Xilinx and technology partner Seiko-Epson (Fujimi, Japan) specifically for high-performance in-system programmable CPLDs. By providing process capabilities beyond that of the competing EEPROM technologies, FastFLASH technology enables new CPLD capabilities previously not available.

For instance, FastFLASH technology offers significant advantages over EEPROM technology used in the current generation of in-system programmable CPLDs. By providing a guaranteed endurance of 10,000 program/erase cycles, FastFLASH technology provides up to 100 times the endurance of EEPROM-based CPLDs. The enhanced endurance arises from three key differences over EEPROM technology. First, the tunnel oxide is 100 Angstroms thick (vs. 80 Angstroms for EEPROM). This allows better process control of oxide quality—a key factor in endurance. Second, the program and erase operation requires only 10 MV/cm, compared with 15-20 MV/cm for EEPROM. The lower electric field makes FastFLASH immune from tunnel oxide breakdown, which is the major cause of endurance failure in EEPROM cells. Finally, the programming time of 100 microseconds is substantially less than the five to ten milliseconds required for EEPROM. This lessens the exposure of high electric fields to the FastFLASH cell.

In addition, the FastFLASH cell size is three times smaller than the comparable EEPROM cell, which allows significantly more routing switches in less die area. CPLD EEPROM cells require separate programming device structures in addition to the control transistor. In contrast, the

FastFLASH technology allows a single merged flash transistor that performs the functions of the separate programming structures, resulting in a small cell area. This contributes to the superior routing characteristics of FastCONNECT over other switch matrix architectures. The FastFLASH cell is shown in Figure 4.

FastFLASH technology is compatible with the industry-leading flash memory processes and is optimized for high-performance logic circuitry. The FastFLASH programming cell was specially developed to provide high switching performance as well as built-in "erase Vt control" to simplify on-chip programming and erase. By including a select transistor to limit the cell Vt, the over-erase problem is eliminated. (See Figure 5.) The result is a high yielding, high performance CPLD technology with enhanced endurance compared with existing EEPROM technologies.

The XC9500 Family

The XC9500 architecture was developed to accommodate the needs of leading-edge applications in telecom, industrial control, and data processing applications. Pin-to-pin propagation delays as fast as five ns.

The XC9500 family consists of nine members ranging in density from 800 to over 12,000 usable gates. (See the table below.) All devices within the family are pin-compatible. This allows user flexibility in selecting the optimal density in each package type.

Device	Macrocells	Usable Gates	Tpd	Registers	Availability
XC9536	36	800	5	36	1Q96
XC9572	72	1,600	7.5	72	2Q96
XC95108	108	2,400	7.5	108	Now
XC95144	144	3,200	7.5	144	3Q96
XC95180	180	4,000	10	180	3Q96
XC95216	216	4,800	10	216	1Q96

XC95288	288	6,400	10	288	2Q96
XC95432	432	9,600	12	432	4Q96
XC95576	576	12,800	15	576	4Q96

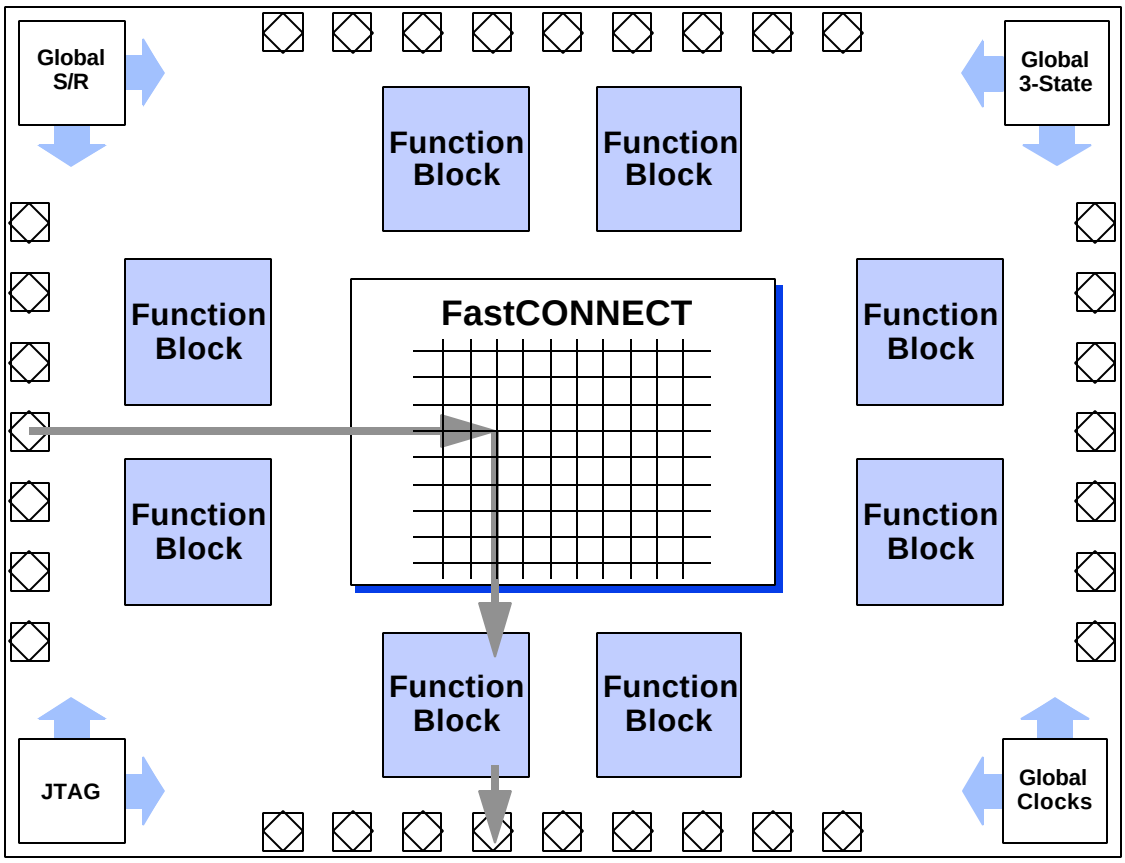

Figure 1. FastCONNECT switch matrix.

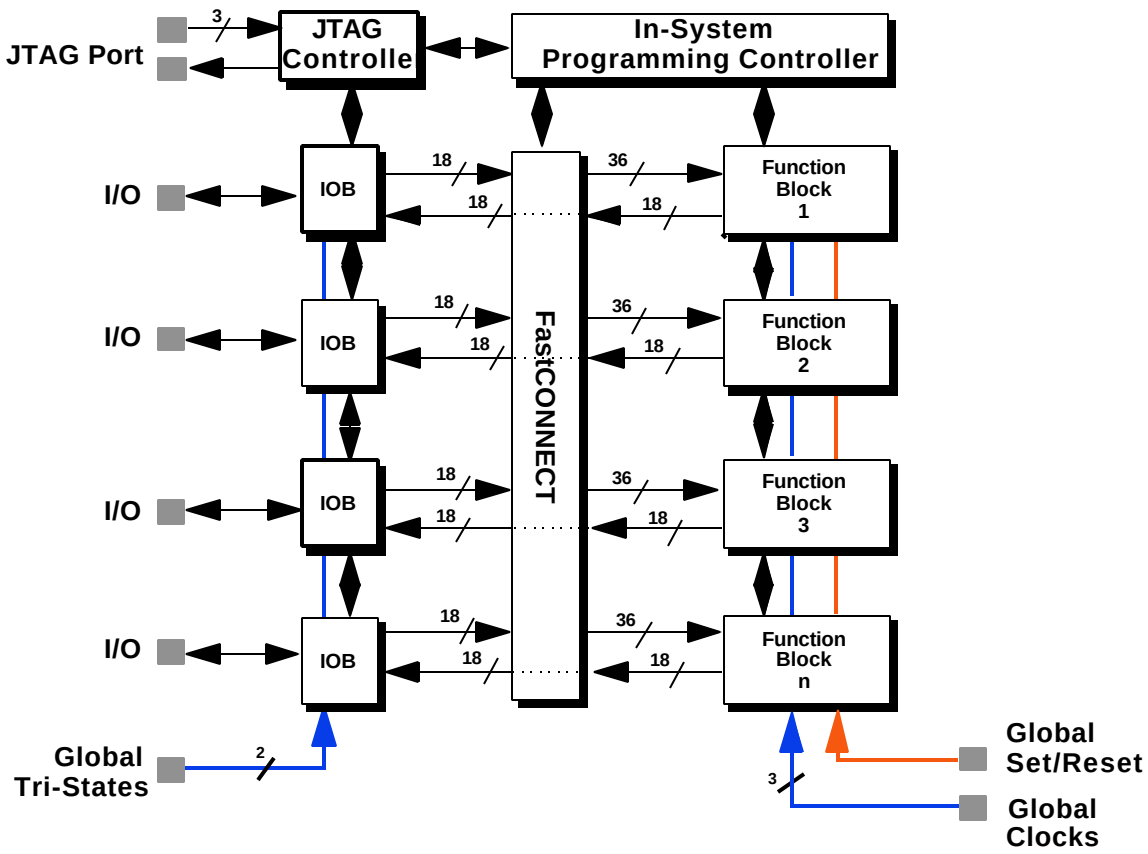

Figure 2. XC9500 block diagram.

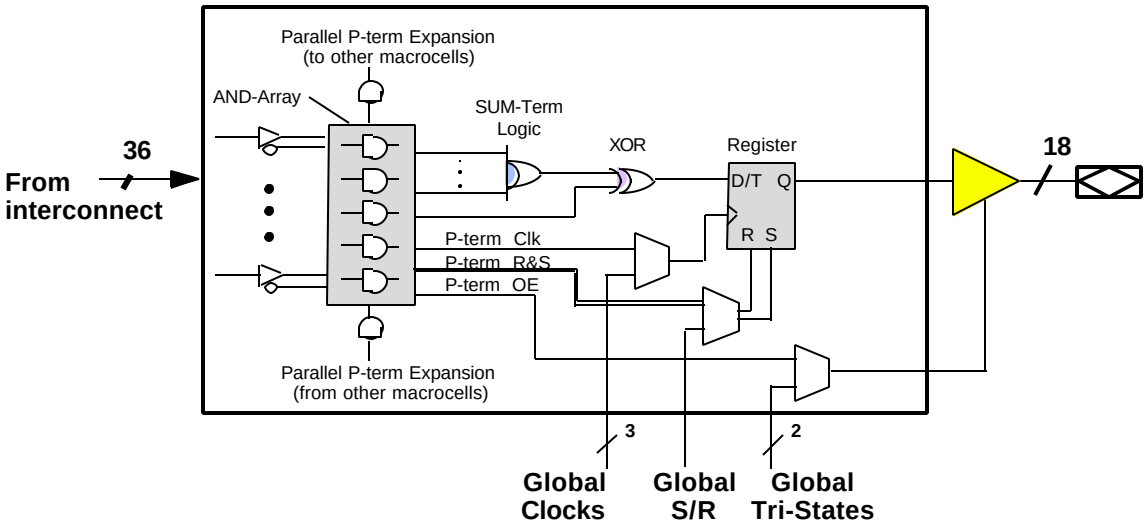

Figure 3. XC9500 macrocell.

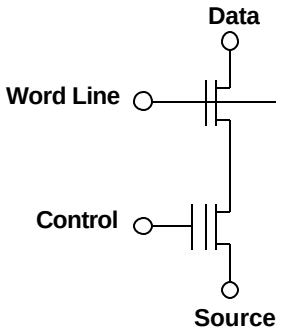

Figure 4. FastFLASH cell.

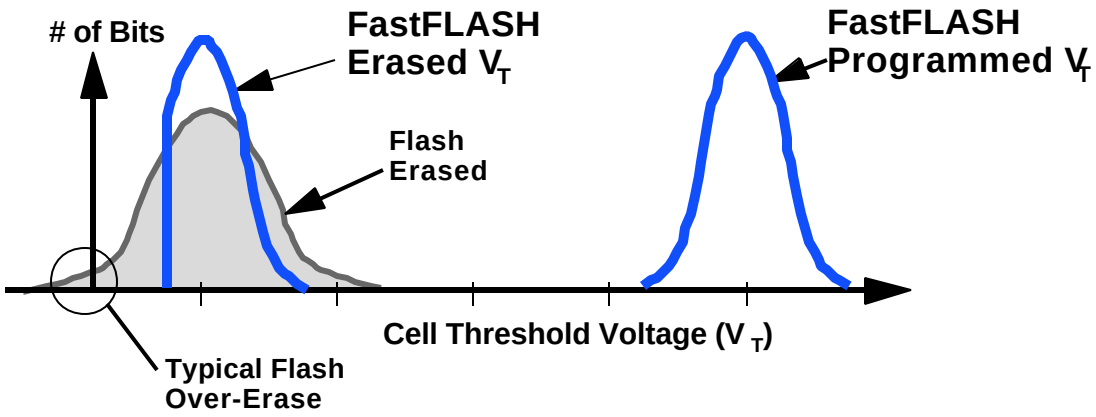

Figure 5. Threshold voltage distribution.